



**CDC® CARD READER/LINE PRINTER
CONTROLLER
FH301-A**

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE REFERENCE/MAINTENANCE MANUAL

[illegible]

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
CY117-B	01 02		
FH301-A	01 02 03 04	14101 14101 14149 14226	
YA117-B	01 02		Clears data status on each feed function.

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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PREFACE

This manual provides reference, programming, and maintenance information for the CONTROL DATA® FH301-A Card Reader/Line Printer Controller, I/O cables and finalization kits.

This manual is intended to serve programmers and customer engineers who require detailed machine-level information about the card reader/line printer controller. Detailed information regarding system-level programming

and maintenance is provided by the reference manual for each system.

Additional card reader and line printer information is contained in the reference and hardware maintenance manuals for the specific equipment.

The following documents will be helpful to the reader:

<u>Publication</u>	<u>Publication Number</u>
Basic Micro-Programmable Processor Hardware/Reference Maintenance Manual	39451400
CB104, FC109, FC539, FH301 Card Reader Subsystem Field Repair Guide	60475031
CL408, CL411, FC109, FC539, FH301 Line Printer Subsystem Field Repair Guide	60475032
CT103, CT105, CT106, FC109, FC539, FH301 Line Printer Subsystem Field Repair Guide	60475033
CYBER 18 - 05/10 Computer Systems Hardware Maintenance Manual, Volumes 1 and 2	96767500 96767600
CYBER 18 Computer Systems with Core Memory Installation Manual	39451500
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
CYBER 18 Processor with Core Memory (Macro Level) Hardware Reference Manual	88973500
CYBER 18 Processor with MOS Memory (Macro Level) Hardware Reference Manual	96768300
Operational Diagnostic System (ODS) Version 1 Reference Manual	39452100
Operational Diagnostic System (ODS) Version 2 Reference Manual	96768410

WARNING

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference with radio communications. It has been tested to comply with the limits for Class A peripheral computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

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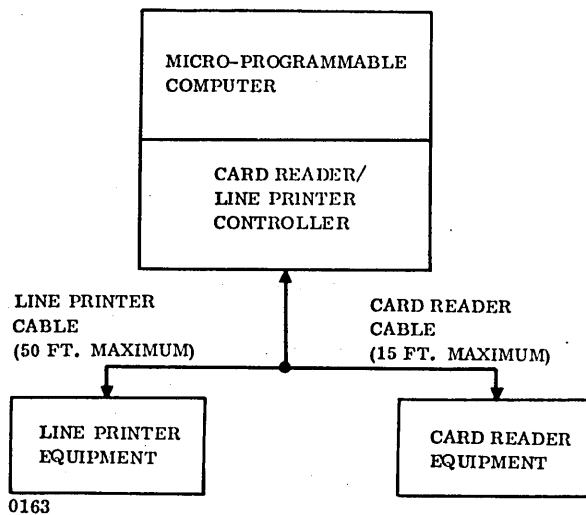
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The card reader/line printer (CR/LP) controller operates with one card reader and/or one line printer. The CR/LP controller is designed for use with any of the CDC® Micro-Programmable Computer Family of processors that provides the proper address, data, and control signals. Input/output commands that are transmitted via the address and data lines initiate and control card reader input and line printer output; they also enable the generation of interrupts when the specified conditions exist. A test mode capability enables the controller to read line printer output data back as card reader input data for diagnostic purposes.

FUNCTIONAL DESCRIPTION

Communication between the CR/LP controller and the computer is by way of a 16-bit device address and command word, a 16-bit input/output function word, and control signals. The card reader interface consists of a 12-bit data word and control signals, while the line printer interfaces with the central processing unit (CPU) via an eight-bit data word, a parity bit, and control signals. All CR/LP controller interface control signals are described in detail in section 4. Figure 1-1 shows the CR/LP controller configuration location within a typical system.



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Figure 1-1. Card Reader/Line Printer Equipment Configuration

CARD READER CONTROLLER

The card reader controller receives a 12-bit data word from the card reader with each data bit corresponding to a card row. Each 12-bit data word equates to a punch card column. During a data transfer operation, the card reader inputs one column of data at a time to the controller. Data punched on the card can be Hollerith, binary coded, or any other desired format. The card reader controller performs no operation on the data except, during a CPU deadstart operation, a parity bit is added to the data that is being input to the computer. The rate at which the controller sends data to the computer is determined by the speed at which the card reader reads cards.

Card reader error conditions are sensed by the controller and provided, upon request, as status to the computer.

LINE PRINTER CONTROLLER

For line printer output, the controller receives data from the computer as an eight-bit word. Each eight-bit word represents a print or control character to the line printer. The line printer controller is transparent to the computer and the line printer since it does not alter the data word. The rate at which the controller sends data to the printer is determined by the computer program and the line printer speed.

Line printer error conditions are sensed by the controller and provided, upon request, as status to the computer.

TEST MODE

The CR/LP controller has a supplementary operating mode called test mode. In test mode, data and control signals are switched in such a way that each controller can be used to test the other. With proper programming, all input/output (I/O) signals and most internal controller functions and status can be tested independently of the peripheral devices.

PHYSICAL DESCRIPTION

The CR/LP controller is constructed utilizing a combination of small-scale integration (SSI) and medium-scale integration (MSI) circuits. Both the card reader and line printer controller are contained on one 11 by 14 inch three-layer printed circuit board. The controller is housed in one of the A/Q input/output card slots of the main computer chassis. Blowers, which are a part of the main computer chassis, provide forced-air cooling for the CR/LP controller.

Physical and environmental requirements of the CR/LP controller are:

Power: +5 vdc at 3.1 amperes

Temperature: 40°F to 120°F (4.4°C to 48.9°C) ambient room temperature

Humidity: 10 to 90 percent relative humidity with no condensation

Warm-Up Time: None

Non-Operating Environment

Temperature: -30°F to 150°F (-34.4°C to 65.6°C)

Humidity: 5 to 95 percent relative humidity with no condensation

The card reader/line printer controller interfaces with a micro-programmable type computer. Operation of the card reader/line printer controller is controlled by a 16-bit address and command word transmitted from the CPU's Q register, combined with a 16-bit function word from the CPU's A register. These I/O commands are translated by the controller into card reader and line printer communication and data signals. Although the card reader and line printer controllers share common circuitry, their operation is described separately.

CARD READER

The address and I/O command word intended for the card reader is formatted as shown in figure 2-1.

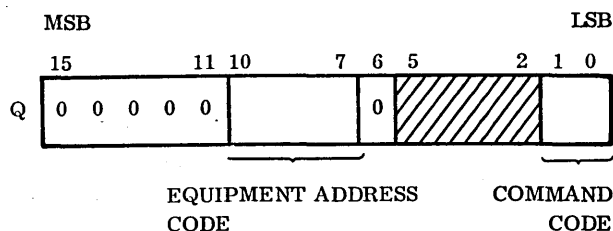


Figure 2-1. Address/Command Format Word (Card Reader)

Bits 7 through 10 of the Q register define the card reader equipment address code and must correspond to the code selected by the four equipment select jumpers. The location of the equipment select jumpers in the controller is shown in figure 5-1. An equipment number is selected by jumpering the equipment number bits to a logical 1 or a logical 0, as shown in figure 2-2.

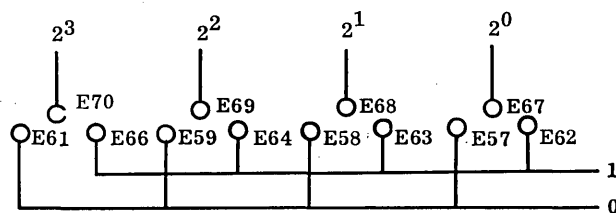


Figure 2-2. Card Reader Equipment Code Selection Jumpers

Q register bits 0 and 1 define a command code that, when accompanied by an equipment code and either a read or write signal, selects the card reader controller operation. Table 2-1 lists the conditions of bits 0 and 1 along with the card reader controller operation selected by the read and write signals.

TABLE 2-1. CARD READER CONTROLLER COMMANDS

Command		Input (Read)	Output (Write)
Q01	Q00		
0	0	Data transfer	Illegal
0	1	Director status 1	Director function
1	0	Illegal	Test mode
1	1	Director status 2	Illegal

Address bits 6 and 11 through 15 must be all zeros while bits 2 through 5 are ignored. All illegal commands are rejected (external reject) by the controller.

The format of the data word in the A register during an input or output operation is determined by the type of operation being performed. Q register bits 0 and 1 determine whether the CPU's A register is to transmit data to or receive data from the controller.

DIRECTOR FUNCTION (Q=xxx1)

When bit 0 in the CPU's Q register is set and bit 1 is clear, an output from the A instruction identifies this operation as a director function. The equipment address defined by Q register bits 8 through 10 must correspond to the card reader equipment code selected in the controller. A bit is set in the A register's data word to specify each of the I/O functions to be performed, as shown in figure 2-3.

Note that for the director function, two or more function bits can be set in the same I/O function word. The director functions are described below.

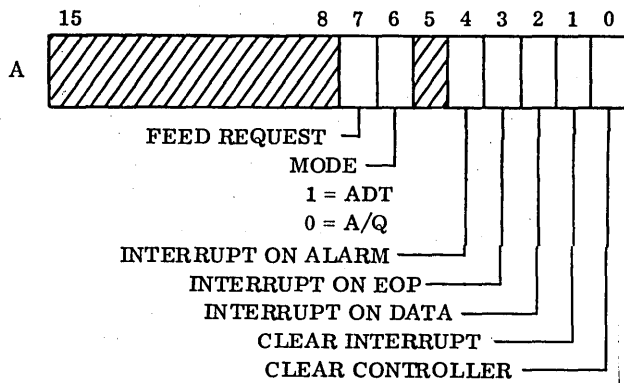


Figure 2-3. I/O Function Word (Director Function Command)

Clear Controller

If set, A register bit 0 causes the controller to clear all interrupt requests, interrupt responses, and alarm conditions. This function is subordinate to all other function codes. The controller accepts and executes a clear controller function if it is not ready, provided that no other function bit except bit 1 is selected at the same time. Care should be exercised in using the clear controller function while the card reader is busy.

Clear Interrupt

If set, A register bit 1 clears all interrupt requests and responses. This function is subordinate to all interrupt request bits (2, 3, and 4) in that it cannot prevent the setting of new interrupts.

Interrupt on Data

If set, A register bit 2 enables an interrupt from the controller when it has data ready to be input by the computer. The interrupt request and response is cleared by a master clear, clear controller, clear interrupt, or a card reader feed director function. When the response is cleared by bit 0 (clear controller) or bit 1 (clear interrupt), the request may be re-enabled in the same operation if bit 2 (interrupt on data) is also selected.

When this interrupt is requested either before or after a feed command but before a data transfer from the card reader, the response signals the computer that card reader data is ready. The data transfer can take place without re-enabling or clearing this interrupt response. Following the data transfer, the interrupt response is removed until the card reader again has data ready.

Interrupt on EOP

If set, A register bit 3 selects the end-of-operation (EOP) interrupt request. When selected, the EOP interrupt occurs when the last column of data has been read and the card has passed through the read station of the card reader. No interrupt response occurs for an operation that was completed before the selection was made. The interrupt request and response can be cleared by a master clear or by setting function bit 0 or 1 while bit 3 is a 0. When the response is cleared by function bit 0 or 1, the request is re-enabled in the same operation if bit 3 is set.

Interrupt on Alarm

If set, A register bit 4 enables an interrupt when an alarm condition exists. An alarm indicates the presence of an abnormal condition. Abnormal conditions include those that cause the card reader to go into a not ready condition as well as one that allows the card reader to remain ready. Conditions causing the card reader to become not ready include manually deactivating the on-line switch, the input hopper is empty, the output stacker is full, a feed failure, a card motion failure, a read alert (failed light or dark check), and a power supply fault. Lost data causes an abnormal condition but does not result in the card reader going into a not ready state.

An alarm condition that exists at the time an interrupt request is made immediately provides a response. When an alarm condition does not exist at the time of the interrupt request, the interrupt response is provided when an alarm condition is detected.

The interrupt request and response is cleared by a master clear, clear controller, or clear interrupt. When the response is cleared by a clear controller (bit 0) or clear interrupt (bit 1), the request is re-enabled in the same operation when interrupt on alarm (bit 4) is also selected.

ADT Mode

If set, A register bit 6 directs the card reader controller to operate in the auto-data transfer (ADT) mode. If operating in the ADT mode, the controller generates a micro interrupt when the data interrupt condition occurs. If either or both of the other interrupts are enabled (EOP or alarm), only a macro program interrupt occurs.

When the micro interrupt is generated, the CPU, upon recognizing it through its internal firmware program, causes data to be transferred to an input buffer in macro memory. This input operation is transparent to the macro program. At the controller, the ADT mode of input functions identically to standard macro program A/Q input operations.

ADT mode operation is cleared by a master clear or by a director function with A register bit 6 equal to 0.

Feed Request

If set, A register bit 7 directs the card reader to initiate a one-card feed cycle. If a second feed request is issued before EOP is sensed for the first read cycle, data transfer is stopped and a new card is fed to the read station. Additionally, no EOP condition is generated for the first card and data input resumes with the first column of the new card. A feed request automatically clears the data status flag.

DIRECTOR STATUS 1

When Q register bit 0 is set and bit 1 is clear, an input to the A (read) instruction defines this operation as a director status 1. The equipment code defined by Q register bits 7 through 10 must correspond to the card reader equipment code selected in the controller. The controller always replies to a director status 1 request by transferring card reader status to the A register. The format of the data word read into the A register is shown in figure 2-4.

The status responses are described below.

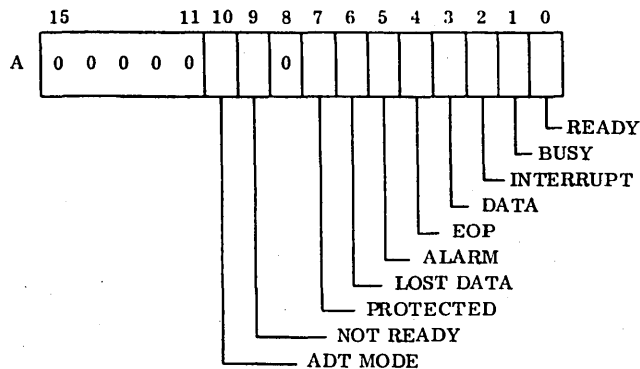


Figure 2-4. Data Word Received
(Director Status 1)

Ready

If set, bit 0 indicates that the card reader is operational. The ready condition must exist before the card reader can operate. The following requirements must be met to produce a card reader ready condition:

- All power supplies are operating.
- Input hopper is loaded.
- Output stacker is not full.
- There is no card jam condition.
- No read alert condition exists.

When any of the above conditions do not exist, manual intervention by the operator is required to correct the malfunction.

Busy

If set, bit 1 indicates that the card reader is busy during a read cycle that was initiated and has not yet completed. The busy condition is cleared at the end of the card cycle or by a clear controller director function.

Interrupt

If set, bit 2 indicates that an interrupt response has been generated by the card reader. Status bits 3, 4, and 5 define the interrupt that occurred.

Data

If set, bit 3 indicates that the controller data register contains information ready for transfer to the computer. If interrupt on data was selected, this status bit also indicates that the interrupt occurred. The status and interrupt conditions are cleared automatically upon completion of the data transfer.

End-of-Operation

If set, bit 4 indicates that the card reader has completed a read cycle (81st column time). If EOP interrupt was selected, this status bit indicates that the interrupt has occurred. EOP status is cleared by a master clear, the start of the next read cycle, or a clear controller director function.

Alarm

If set, bit 5 indicates that an alarm condition exists. The alarm can be caused by either a lost data condition or a card reader malfunction as described by the interrupt on alarm director function. This status bit is cleared by a master clear, a clear controller director function, or a feed director function, provided that the cause of the alarm has been corrected.

Lost Data

If set, bit 6 indicates that data was not transferred to the computer before the next column of data was ready for input. All subsequent columns of data on the card are lost since the controller rejects any further data transfer commands until the EOP status is sensed. Lost data status is cleared by a master clear, a clear controller director function, or a feed director function.

Protected

If set, bit 7 indicates that the controller protect jumper is installed, and the controller is therefore operating in protected mode.

Not Ready

Bit 9 is the logical complement of the ready status (bit 0).

ADT Mode

If set, bit 10 indicates that the controller is currently operating in the auto-data transfer mode.

DIRECTOR STATUS 2

When Q register bits 0 and 1 are both set, an input to the A instruction defines this operation as a director status 2. The equipment code defined by Q register bits 7 through 10 must correspond to the card reader equipment code selected in the controller. The controller always responds to a director status 2 request by transferring the card reader error status to the A register in the format shown in figure 2-5.

The status responses are described below.

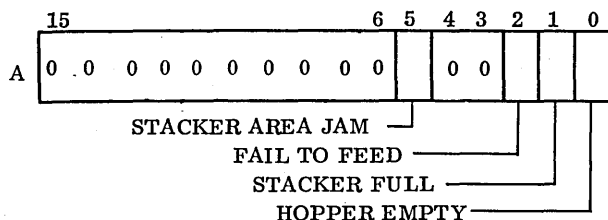


Figure 2-5. Data Word Received
(Director Status 2)

Hopper Empty

If set, bit 0 indicates that the card reader's input hopper is initially empty or is empty after the last card has been read.

Stacker Full

If set, bit 1 indicates that the card reader's output stacker is full and that the last card fed has been read.

Fail to Feed

If set, bit 2 indicates that the card reader was not able to feed the next card from the deck after two feed attempts.

Stacker Area Jam

If set, bit 5 indicates a jam in the card path from the read station to the stacker.

DATA TRANSFER

When Q register bits 0 and 1 are both clear, an input to the A instruction initiates a single column data transfer. The equipment code defined by Q register bits 7 through 10 must correspond to the card reader equipment code selected in the controller. During data transfer mode, data from the card column read is transferred to bits 0 through 11 of the A register data word as shown in figure 2-6. The numbers in the data word bit positions indicate the card row associated with each bit.

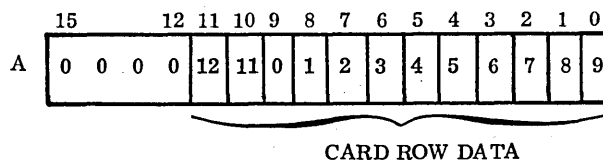


Figure 2-6. Data Word (Data Transfer Format)

Before initiating data transfers, a card must first be picked and fed. This is accomplished by executing a director function ($Q = xxx1_{16}$) with feed request ($A07 = 1$). Following this operation, execution of 80 successive data transfers result in the reading of all 80 columns of data on the punch card to the CPU's A register.

Data transfer commands are accepted only when all of the following conditions exist:

- The card reader is ready.
- Data Status (bit 3) is a logical 1.
- No program protect violation exists.
- Alarm status (bit 5) is a logical 0.

If interrupt on data was selected, each data transfer clears the data status and the interrupt response.

ADT OPERATION

ADT mode may be initiated after executing a macro DMI instruction (refer to the applicable processor hardware reference manual) and setting up the ADT table in main memory.

ADT mode data transfers from the card reader can then be initiated as follows:

Director Function = $00D8_{16}$ (ADT mode, feed, enable alarm, and EOP interrupts)

This causes the card reader to initiate a feed cycle, enable the micro interrupt, and input the card data to main memory as defined by the ADT table parameters. It also enables the macro interrupts that signify the completion of the data transfer.

TEST MODE

When Q register bit 0 is clear and bit 1 is set, an output from the A instruction selects the controller for test mode operation. The equipment code defined by Q register bits 7 through 10 must correspond to the card reader equipment code selected in the controller. When bit 0 of the function word in the A register is set, both the card reader controller and the line printer controller go into a self-test mode. Although test mode is selected by addressing the card reader controller, this mode puts both the line printer and the card reader controllers into a test configuration. One controller cannot be tested in this mode without the other.

Test mode operation is cleared by either a master clear or a test mode function with A register bit 0 clear.

This command is accepted only if both controllers are not busy. Figure 2-7 shows the data word format used to select test mode.

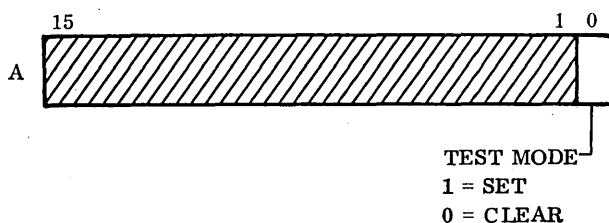


Figure 2-7. I/O Function Word (Test Mode Format)

LINE PRINTER

The address and I/O command word used to define a line printer operation is in the format shown in figure 2-8.

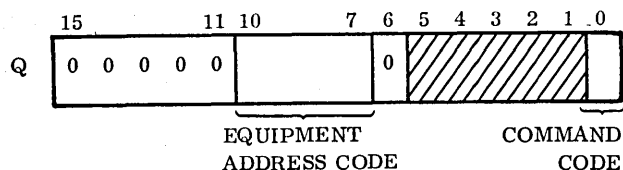


Figure 2-8. Address/Command Word (Line Printer Format)

Bits 7 through 10 of the Q register define the line printer equipment code and must correspond to the code selected by the four equipment select jumpers. The location of the equipment select jumpers within the controller is shown in figure 5-1. An equipment jumper is selected by jumpering the equipment number bits to a logical 1 or a logical 0 as shown in figure 2-9.

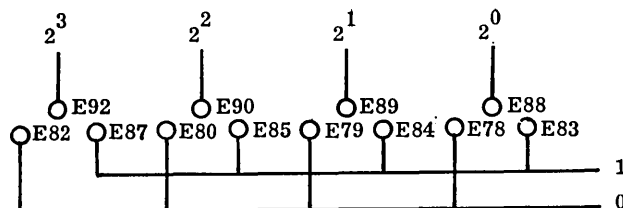


Figure 2-9. Line Printer Equipment Code Select Jumpers

Q register bit 0 defines a command code that, when accompanied by an equipment code and either an input or output to the A instruction, selects the operation to be performed by the line printer. Table 2-2 lists the operations selected by bit 0 during the read or write operation.

TABLE 2-2. LINE PRINTER CONTROLLER COMMANDS

Q00	Input (Read)	Output (Write)
0	Illegal	Data transfer
1	Director status	Director function

Q register bits 6 and 11 through 15 must be all zeros, while bits 1 through 5 are ignored. All illegal commands are rejected (external reject) by the controller.

The format of the I/O function word in the A register during a read or write operation is determined by the type of operation being performed. Q register bit 0 determines whether the data word in the A register is output data, a function command, or status.

DIRECTOR FUNCTION

When Q register bit 0 is set during an output from the A instruction, the data word in the A register is used to determine the director functions. The equipment code defined by Q register bits 7 through 10 must correspond to the line printer equipment code selected in the controller. A bit is set in the A register word to specify each director function to be performed, as shown in figure 2-10.

The director functions defined by the set condition of the CPU's A register bits are described below.

Clear Printer

If set, bit 0 clears all control, interrupt requests, interrupt responses, and alarm conditions. This function is subordinate to all other functions except the print function. The printer must be ready and not busy to execute the clear printer function.

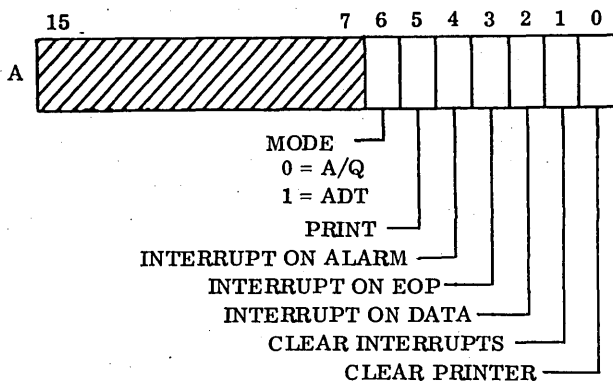


Figure 2-10. I/O Function Word
(Director Function Format)

Clear Interrupts

If set, bit 1 clears all interrupt enables (requests) and interrupts (responses). This function is subordinate to all input request bits (2, 3, and 4) in that it cannot prevent the setting of new interrupts.

Interrupt on Data

If set, bit 2 enables an interrupt from the controller that indicates that the printer is ready to receive data. When this interrupt is enabled prior to initiating a data transfer to the printer, the interrupt response signals the computer that the printer is ready to receive data. The data transfer can take place, or a print command may be issued, without re-enabling or clearing this interrupt response. Following a data transfer or print cycle, the interrupt is automatically removed until the printer is again ready to receive data.

The interrupt enable and interrupt are cleared by a master clear or by either the clear printer or the clear interrupts function when the interrupt on data function is not selected. When the response is cleared by the clear printer or clear interrupts function, the request is re-enabled in the same operation if the interrupt on data function is also selected.

The clear controller function requires 5 microseconds, so it should not be immediately followed by a data transfer or print direction function.

Interrupt on EOP

If set, bit 3 enables an interrupt on completion of a print operation. When the EOP interrupt is selected before or during a print cycle, the response occurs when the operation has completed. No interrupt response occurs for an operation that has completed before the EOP interrupt selection was made.

Interrupt on Alarm

If set, bit 4 enables an interrupt when an alarm condition exists. If an alarm condition exists at the time an interrupt on alarm request is made, the interrupt response is generated immediately. When the alarm condition does not exist at the time of the interrupt request, the interrupt response is generated when an alarm condition is detected. Alarm conditions are divided into two types: those that cause the printer to go not ready and those malfunctions during which the printer remains ready. Conditions that cause the printer to become not ready and require operation intervention include paper out, paper tear, fuse alarm, open interlock, and power supply fault. Malfunctions that allow the printer to remain ready are transmission parity error, illegal character code transferred into printer memory, image counter out of sync with the train array, train running at an incorrect speed, image memory out of sync, and image memory out of sync, and image memory being loaded. All of these alarm conditions do not apply to all line printers since some printers do not contain the features that would generate these errors. The interrupt enable and interrupt is cleared by a master clear, clear controller, or a clear interrupt director function. When the interrupt enable or interrupt is cleared by a clear controller (bit 0) or a clear interrupt (bit 1), the request is re-enabled in the same operation if interrupt on alarm (bit 4) is also selected.

Print

If set, bit 5 directs the printer to print the contents of its memory that were loaded previously through data transfer operations. This initiates a print command and completion of a line of print. During a print cycle, the ready for data status (bit 3) is dropped.

ADT Mode

If set, bit 6 directs the printer controller to operate in the auto-data transfer (ADT) mode. If operating in ADT mode, the controller generates a micro interrupt when the data interrupt condition occurs. If either or both of the other interrupts are enabled (EOP or alarm), only a macro program interrupt occurs. When the micro interrupt is recognized by the CPU, its internal firmware program causes data to be transferred from an output data buffer in macro memory to the printer's memory. This input/output operation is transparent to the macro program. At the controller, the ADT output mode functions identically to standard macro program A/Q output operations.

When ADT mode is used with the line printer, the controller limits the output data rate to approximately 13.3 kHz. This slowdown prevents the line printer controller from monopolizing the CPU during the data transfer.

ADT mode is cleared by a master clear or by a director function with A register bit 6 clear.

DIRECTOR STATUS

When Q register bit 0 is set and an input to the A instruction is executed, then a director status operation is selected. The equipment code defined by Q register bits 7 through 10 must correspond to the line printer equipment code selected in the controller. The controller always replies to a director status request by transferring line printer status to the A register. Figure 2-11 shows the format of the read data word in the CPU's A register.

The status responses defined by the associated A register bit being set are described below.

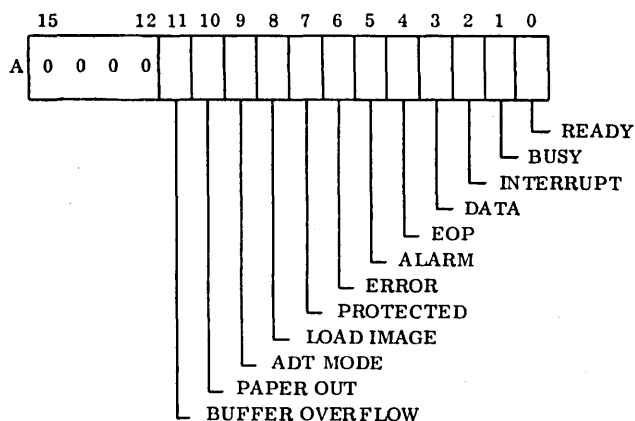


Figure 2-11. Data Word Received
(Director Status Format)

Ready

If set, bit 0 indicates that the printer is operational and on-line. The ready condition must exist before the printer can operate. The following requirements must be met to produce a line printer ready condition:

- All power supplies are operating.
- Hammer fuses are intact.
- Paper is present.
- The drum gate or tray array gate is latched.
- No paper motion fault exists.
- Image memory is loaded or the load image indicator is illuminated (only on printers with image memory).

Busy

If set, bit 1 indicates the line printer is busy during a print cycle.

Interrupt

If set, bit 2 indicates an interrupt response has been generated by the printer. Status bits 3, 4, and 5 define the interrupt that occurred.

Data

If set, bit 3 indicates the printer is ready to receive data. If interrupt on data was selected, this status bit also indicates that the interrupt has occurred.

EOP

If set, bit 4 indicates that the printer has completed a print cycle. If the EOP interrupt was selected, this status bit also indicates the EOP interrupt has occurred. The EOP status bit is the logical complement of the busy status (bit 1).

Alarm

If set, bit 5 indicates that an alarm condition exists. The alarm can be caused by either an error (status bit 6) or a printer malfunction as described by the interrupt on alarm director function. This status bit is cleared by a master clear or a clear printer, data transfer, or a print director function, provided that the cause for the alarm has been corrected.

Error

Bit 6, depending on the printer being used, indicates a parity error, synchronization error, or compare error occurred. The printer remains ready when any of these conditions exists. This status bit is cleared by a master clear or a clear printer, data transfer, or print director function.

Protected

If set, bit 7 indicates that the controller protect jumper is in place. The controller is therefore operating in a protected mode.

Load Image

Status bit 8 is used only when the controller is connected to a line printer that contains an image memory.

If set, bit 8 indicates that the START pushbutton has been depressed, no fault conditions exist, and the fill image pushbutton was depressed on the printer.

The load image status indicates the printer will place the next 288 data characters into the image memory. If a parity error occurs, no further transmission takes place until a master clear or clear printer director function is issued. This status bit is cleared upon successful transfer of the 288 data characters,

ADT Mode

If set, bit 9 indicates that the controller is currently operating in the auto-data transfer mode.

Paper Out

When the printer is equipped with the paper out status option, bit 10 indicates that an out-of-paper condition has been detected at the lower tractor switches. Approximately 3 inches of paper normally remain between the bottom edge of the last form and the print station. When this condition occurs, the printer becomes not ready.

Buffer Overflow

When the printer is equipped with the buffer overflow status option, bit 11 indicates that more than the maximum number of characters for a line has been received. This status bit is set during the transfer of the first excess data byte. The buffer overflow status bit is cleared by a master clear or a clear printer or print director function. All overflow characters are responded to, but not stored or printed.

DATA TRANSFERS

When Q register bit 0 is clear, executing an output from the A instruction selects data transfer mode. The equipment code defined by Q register bits 7 through 10 must correspond to the line printer equipment code selected in the controller. During data transfer mode, bits 0 through 7 of the data word contained in the A register are transmitted to the line printer as data. Figure 2-12 shows the data word format during a data transfer operation.

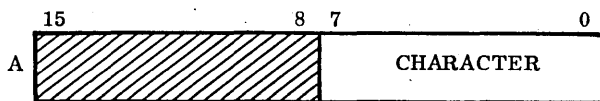


Figure 2-12. Data Word (Data Transfer Format)

Data transfer commands are accepted only when the following conditions exist:

- The printer is ready and not busy.
- Data status (bit 3) is set.
- No program protect violation exists.

The first character of a line is identified as a control character for vertical paper motion and is not printed. The printer must be equipped with the preprint paper motion option. This option causes the paper motion cycle to occur before the print cycle. Paper motion is initiated upon receipt of

the format command (first transmitted character), but the printer does not set the busy status. The remainder of the line is then loaded while the paper advance cycle is in progress. The print cycle occurs after the advance cycle has completed.

If a control character is issued that performs a vertical paper motion, and a clear printer director function is issued immediately thereafter, the busy status is set. The busy status remains set until paper motion stops. Control characters for vertical paper motion are listed in table 2-3.

ADT OPERATION

ADT mode data transfer to the printer must be initiated as follows:

- Director 0041₁₆ (ADT mode, clear printer).
function 1 This conditions the printer for a new line of print and causes the first macro data interrupt.
- Director 0058₁₆ (ADT mode, enable alarm, and EOP interrupts). This enables the macro interrupts that signify the completion of the data transfer.

The above functions must be executed in the sequence shown after first setting up the output data buffer and ADT table and executing a macro DMI instruction (refer to the applicable processor hardware maintenance manual).

PROGRAM PROTECT

The card reader and line printer controllers each has the capability of operating in a protected or unprotected mode, independently of the other controller. Selection of protected mode requires the installation of one jumper for each controller, as shown in figures 2-13 and 2-14.

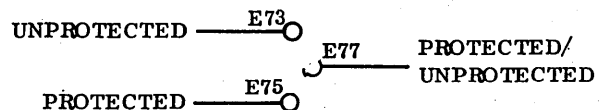


Figure 2-13. Card Reader Protect

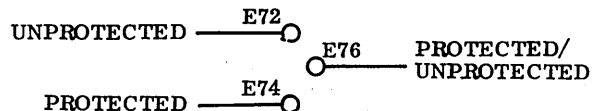


Figure 2-14. Line Printer Protect

TABLE 2-3. PAPER MOTION CONTROL CHARACTERS

Data Bits								Function
07	06	05	04	03	02	01	00	
X	0	X	X	X	X	0	0	Suppress space
X	0	X	X	X	X	0	1	Single space
X	0	X	X	X	X	1	0	Double space
X	0	X	X	X	X	1	1	Triple space
								<u>Vertical Format Control</u>
X	1	X	X	0	0	0	0	Channel 1 (TOF)
X	1	X	X	0	0	0	1	Channel 2 (BOF)
X	1	X	X	0	0	1	0	Channel 3
								.
								.
								.
X	1	X	X	1	0	1	1	Channel 12
X	1	X	X	1	1	0	0	} Illegal as vertical format control
X	1	X	X	1	1	0	1	
X	1	X	X	1	1	1	0	
X	1	X	X	1	1	1	1	

NOTES: 1. X = Don't care

2. When an illegal vertical format control character is issued, it is decoded as if bit 6 = 0.

PARITY SELECTION

The data word interface between the controller and the line printer can be jumper-selected to transmit either odd or even parity. Figure 2-15 shows the jumper connectors used to determine parity. The standard line printer configuration uses odd parity.

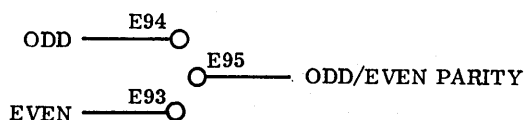
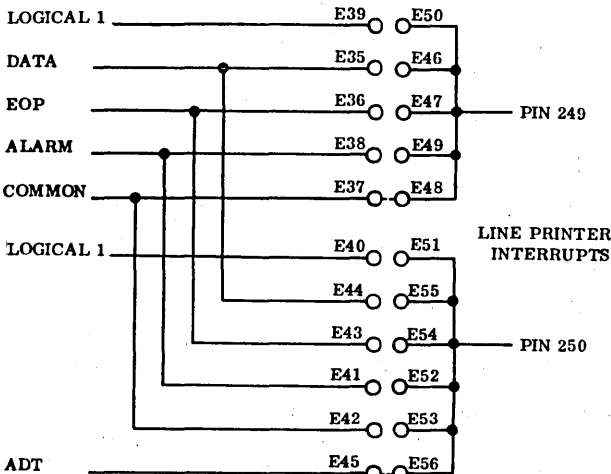
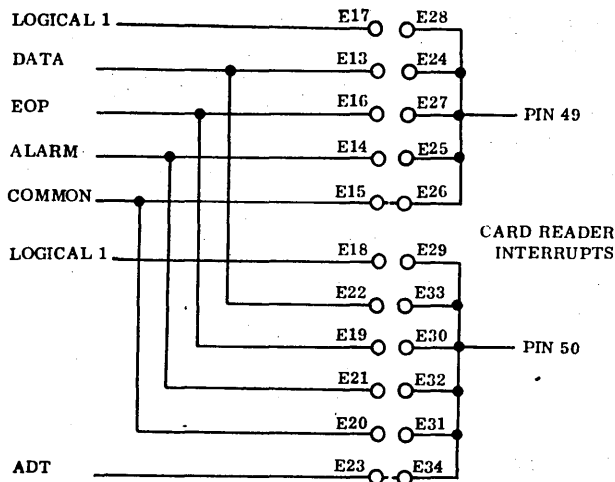


Figure 2-15. Parity Selection

INTERRUPTS

The line printer and card reader controllers each generates five different interrupts. These interrupts are brought to two selection matrices where any two of the five interrupts for each controller may be jumpered to either of two CPU interrupt lines (total of four). When one or more of the four interrupts is not used, it can be disabled within the selection matrix. Interrupt selection requires that one jumper be installed for each interrupt. The jumper connections are shown in figure 2-16.



NOTE: --- INDICATES STANDARD INTERRUPT JUMPERS

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Figure 2-16. Interrupt Selection

Interrupts available from the card reader and line printer controllers are:

- Data interrupt
 - EOP interrupt
 - Alarm interrupt
 - Common interrupt
 - ADT interrupt
- } Macro interrupts
- Micro interrupt

The common interrupt is active whenever any of the data, EOP, or alarm interrupts are active (logical OR), and is normally selected as the macro interrupt.

The ADT interrupt is active only when the controller is operating in ADT mode, the data interrupt condition is present, and no EOP or alarm interrupt exists. The ADT interrupt is cleared by a master clear or a clear interrupt, clear controller, data transfer, or print director function.

ADDRESSING A DISABLED CONTROLLER

Both the card reader and the line printer controllers can be disabled by a jumper selection. The card reader enable jumper is shown in figure 2-17 and the line printer enable jumper is shown in figure 2-18. When disabled, a controller does not respond to any of the 16 available equipment numbers. Therefore, the controller is effectively out of the system from a programming viewpoint.

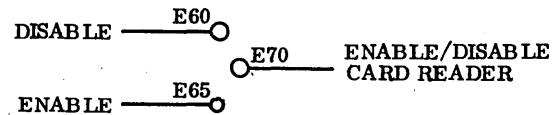


Figure 2-17. Card Reader Enable

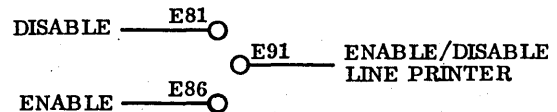


Figure 2-18. Line Printer Enable

During test mode operation, the diagnostic program must be able to address both controllers even if only one is used in the system. To provide this capability, both the line printer and card reader controllers are designed with a special feature that allows a disabled controller to be addressed through the use of Q register address bit 6. The disabled controller provides a normal response when the enabled controller is addressed by its controller's equipment code and bit 6 is set. To address an enabled controller, address bit 6 must be equal to 0.

DEADSTART OPERATION

The card reader controller contains logic to implement a deadstart operation (nonprogrammed data transfer) from the card reader. During deadstart, the controller reads cards at the maximum rate of the card reader.

Deadstart operation is initiated when the deadstart command line from the CPU is activated. The deadstart command line activates when deadstart is selected in the CPU by either a micro program instruction or a remote pushbutton switch. Although the pushbutton switch is not part of the card reader controller, signal conditioning and latching circuitry for the switch is provided by the card reader controller.

The deadstart command line is disabled as a result of a master clear, a micro program instruction, or incoming deadstart data. When deadstart command line goes inactive, the deadstart operation is terminated at the completion of the card currently being read.

During deadstart, Hollerith characters are read from cards one column at a time and converted to equivalent ASCII codes, as shown in table 2-4. Only Hollerith numbers 0 through 9, letters A through O, and the Hollerith + are recognized by the CPU as valid characters. Blank (empty) columns are ignored. Since all 80 card columns are converted to ASCII code, comments are not allowed on the card.

NOTE

Hollerith-to-ASCII conversion occurs within the card reader only during deadstart operation.

Each converted Hollerith character is sent to the CPU as an asynchronous serial data transmission consisting of one start bit, seven data bits, one parity bit, and one or more stop bits. Card reader deadstart data is normally transmitted to the CPU at 9600 baud.

TABLE 2-4. DEADSTART HOLLERITH-TO-ASCII CONVERSION

Hollerith Character	Hollerith Punch (026)	ASCII Code (Hexadecimal)	ASCII Character
0	0	30	0
1	1	31	1
2	2	32	2
3	3	33	3
4	4	34	4
5	5	35	5
6	6	36	6
7	7	37	7
8	8	38	8
9	9	39	9
A	12-1	41	A
B	12-2	42	B
C	12-3	43	C
D	12-4	44	D
E	12-5	45	E
F	12-6	46	F
G	12-7	47	G
H	12-8	48	H
I	12-9	49	I
J	11-1	4A	J
K	11-2	4B	K
L	11-3	4C	L
M	11-4	4D	M
N	11-5	4E	N
O	11-6	4F	O
P	11-7	4C	L
Q	11-8	4C	L
R	11-9	4C	L
S	0-2	32	2
T	0-3	33	3
U	0-4	34	4
V	0-5	35	5
W	0-6	36	6
X	0-7	37	7
Y	0-8	38	8
Z	0-9	39	9

TABLE 2-4. DEADSTART HOLLERITH-TO-ASCII CONVERSION (Contd)

Hollerith Character	Hollerith Punch (026)	ASCII Code (Hexadecimal)	ASCII Character
=, (, \$ * .	8-3	3B	;
	8-4	3C	<
	0-3-8	3C	;
	0-4-8	3C	<
	11-3-8	4C	L
	11-4-8	4D	M
	12-3-8	4B	K
), - + /	12-4-8	4C	L
	11	4C	L
	12	40	@
	0-1	31	
Other miscellaneous common Hollerith punches	8-2	3A	:
	8-5	3D	=
	8-6	3E	>
	8-7	3F	?
	11-0	4C	L
	12-0	40	@
	0-8-2	3A	:
	0-8-5	3D	=
	0-8-6	3E	>
	0-8-7	3F	?
	11-8-2	4B	K
	11-8-5	4E	N
	11-8-6	4F	O
	11-8-7	4C	L
	12-8-2	4A	J
	12-8-5	4D	M
	12-8-6	4E	N
	12-8-7	4F	O

Information for this section is contained in the
CYBER 18 Computer Systems Installation Manual and

in the CYBER 18 Computer Systems Hardware
Maintenance Manuals, listed in the preface.

THEORY OF OPERATION

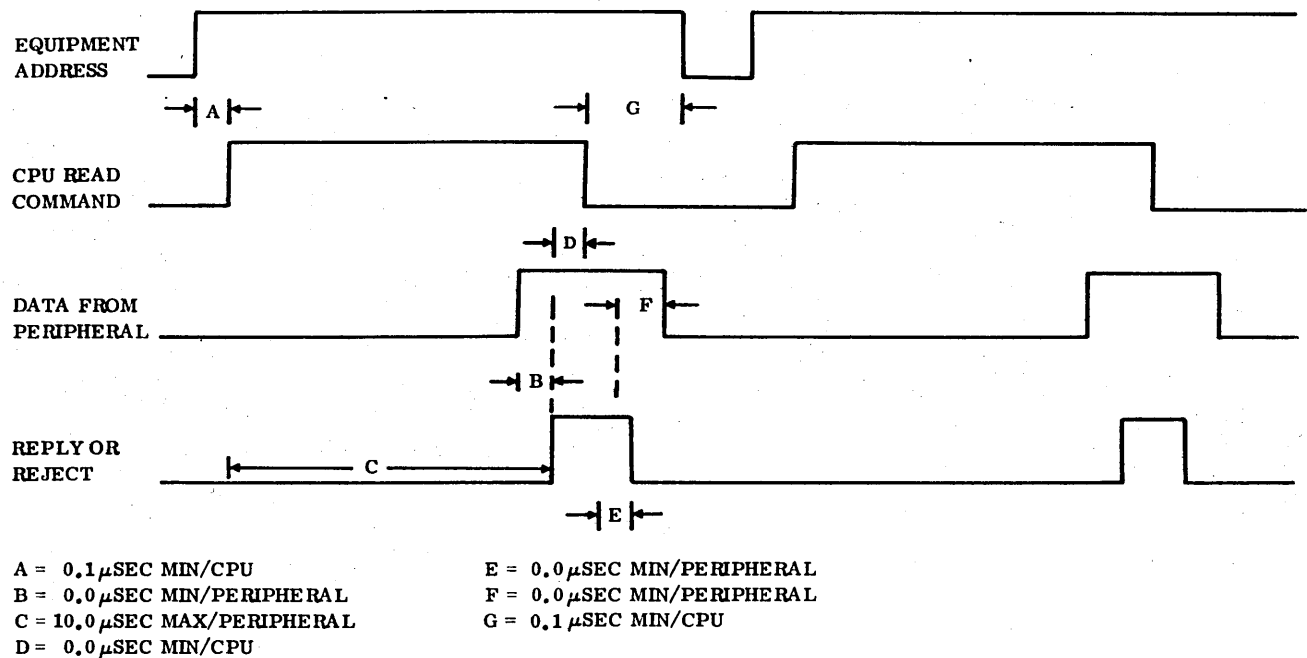
4

The card reader/line printer controller provides an interface between the A/Q channel within the micro-programmable processor and any card reader and/or line printer that meets the controller's signal interface requirements.

During normal operation, the card reader/line printer controller functions as a transparent interface between the micro-programmable processor and the peripheral equipment. In addition to its normal input/output data interface mode, the controller can be operated in either a deadstart or test mode. During deadstart mode, specially punched Hollerith data is read from the card reader, converted to ASCII code, and transmitted serially to the CPU. Test mode provides a means of

turning line printer output data and control signals around to simulate input data and control signals. Figure 5-2, the combined functional block diagram of the card reader/line printer controller, should be referenced during the following descriptions.

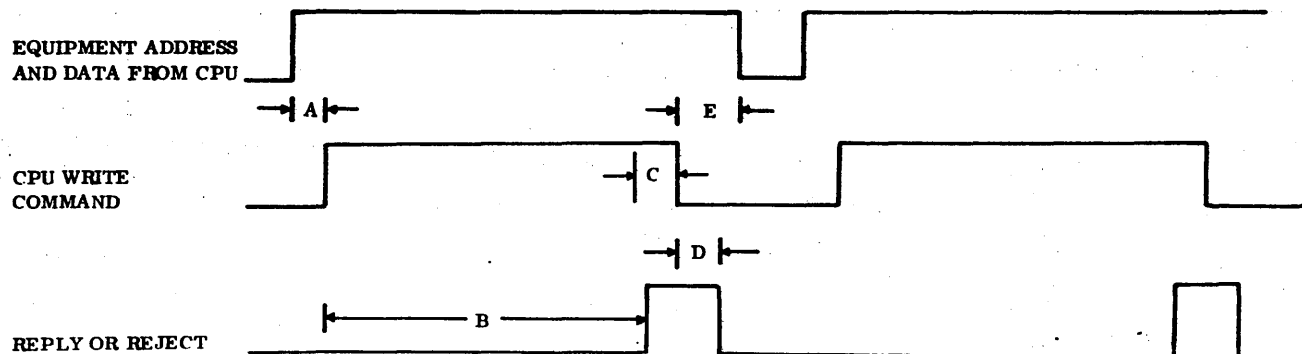
The micro-programmable processor communicates with the card reader/line printer controller by way of the A/Q programmed I/O channel of the CPU. Within the controller, the card reader and line printer each has its own equipment select and peripheral interface control sections, although they share a common A/Q channel interface. Figures 4-1 and 4-2 show the timing relationship of the A/Q channel interface signals.



NOTE: ADDRESS LINES NEED NOT DROP AFTER THE CPU READ COMMAND DROPS, AND IN GENERAL, THEY WILL NOT CHANGE UNTIL THE BEGINNING OF THE NEXT I/O OPERATION.

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Figure 4-1. A/Q Input Operation Timing



A = 0.1 μ SEC MIN/CPU

B = 10.0 μ SEC MAX/PERIPHERAL

C = 0.0 μ SEC MIN/CPU

D = 0.0 μ SEC MIN/PERIPHERAL

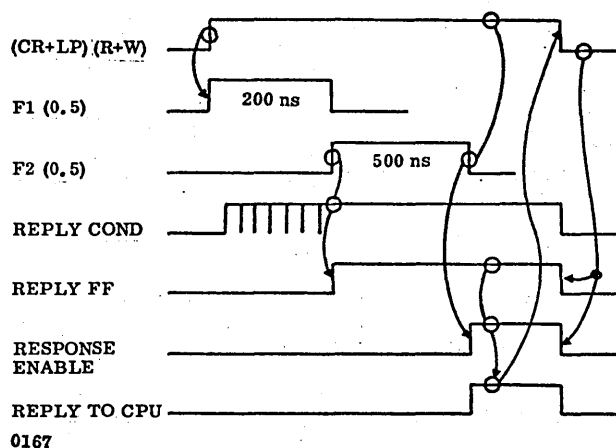
E = 0.1 μ SEC MIN/CPU

NOTE: ADDRESS AND OUTPUT DATA LINES NEED NOT DROP AFTER THE CPU WRITE COMMAND DROPS, AND, IN GENERAL, THEY WILL NOT CHANGE UNTIL THE BEGINNING OF THE NEXT I/O OPERATION.

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Figure 4-2. A/Q Output Operation Timing

Internal timing signals that are generated when the controller recognizes an A/Q input or output command are shown in figure 4-3.



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Figure 4-3. Internal A/Q Interface Timing

The CR/LP controller generates a reply to the CPU to indicate that the controller has accepted the operation. Table 4-1 shows the conditions that generate the reply.

TABLE 4-1. CARD READER/LINE PRINTER REPLY CONDITIONS

Operation	Reply Conditions
Card Reader	
CR Function	WRITE $\bullet$ CRPROTOK (CRRDY + A02 $\bullet$ A03 $\bullet$ A04 $\bullet$ A06 $\bullet$ A07)
CR Status 1	READ (accepted unconditionally)
CR Status 2	READ (accepted unconditionally)
CR Data	READ $\bullet$ CRPRTOTOK $\bullet$ CRLM $\bullet$ CRDSTAT
Set Test Mode	WRITE $\bullet$ CRPROTOK $\bullet$ LPBSY $\bullet$ CRBSY $\bullet$ A00
Clear Test Mode	WRITE $\bullet$ CRPROTOK $\bullet$ A00

TABLE 4-1. CARD READER/LINE PRINTER
REPLY CONDITIONS (Contd)

Operation	Reply Conditions
Line Printer	
LP Function	WRITE ● LPPROTOK (A05 + LDSTAT ● LPRDY ● LPBSY)
LP Status	READ (accepted unconditionally)
LP Data	WRITE ● LPRDY ● LPBSY ● LDSTAT ● LPPROTOK
NOTE: CRPROTOK - CR program protect conditions are met LPPROTOK - LP program protect conditions are met CRRDY - CR ready = 1 LPRDY - LP ready = 1 CRBSY - CR busy = 1 LPBSY - LP busy = 1 CRALM - CR alarm = 1 CDSTAT - CR data = 1 LDSTAT - LP data = 1	

LINE PRINTER CONTROLLER

The equipment number contained in bits 7 through 10 of the address word is compared to the line printer controller's equipment number during a CPU input/output operation. When the controller is enabled and the address word equipment code matches the line printer equipment number jumper selected, address bit 0 and the read/write signal combine to determine the controller's operating mode. When address bit 0 is set during a write operation, the output data word is used as a director function.

When address bit 0 is clear during a write operation, the data word contains output data for the line printer. Director status is input to the data word during a read operation when address bit 0 is set.

The first character in each line output to the line printer is defined as a control character for vertical paper motion and is not printed, except when loading the image buffer of printers that have image buffers. The line printer must be equipped with the preprint paper motion option. This option causes the paper motion cycle to occur before the print cycle. Paper motion is initiated upon receipt of the format command (the first transmitted character). The printer does not set the busy status during paper motion. The line to be printed is loaded while the paper advance cycle is in progress, and the print cycle occurs after the paper advance cycle is complete. If a paper motion control character is immediately followed by a clear printer director function, the busy status remains set until paper motion stops. The line printer format control characters are shown in table 2-3.

The line printer controller is capable of generating either odd or even parity. Parity is determined by the placement of the parity jumper shown in figure 2-15 and must conform to the parity scheme used by the line printer. Normally, odd parity is used.

The line printer controller is capable of generating data, end of operation, alarm, common, and auto-data transfer interrupts. These interrupts are brought to an interrupt selection matrix where any two of the five can be jumpered to either of two CPU interrupt lines.

Basic line printer controller to line printer timing is shown in figure 4-4. The printer requests a character by activating the character request line. The controller responds by placing information on the data lines and activating the

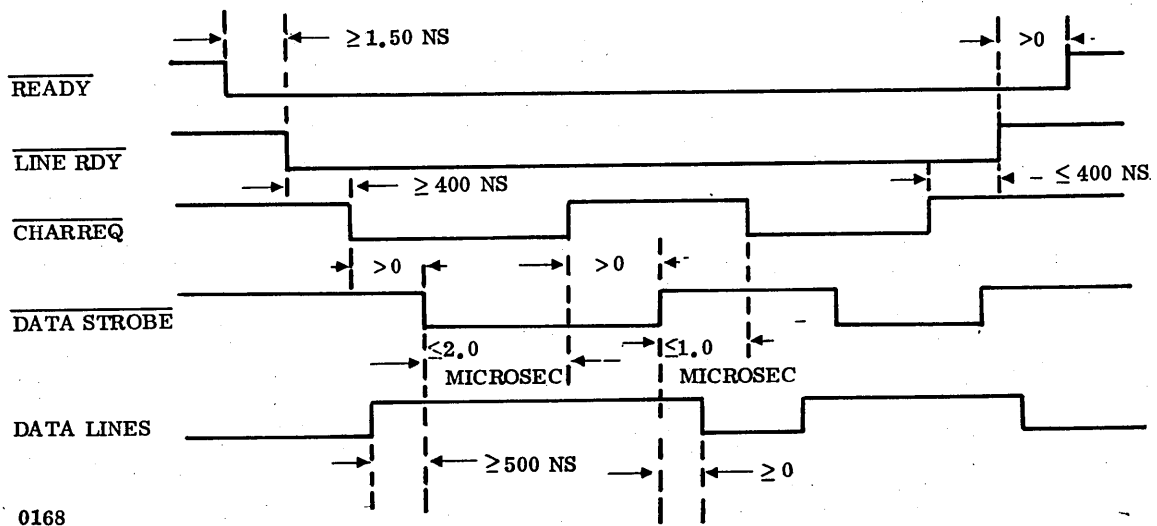


Figure 4-4. Basic Line Printer Input/Output Timing

data strobe line. The printer drops character request when the data byte has been sampled, which in turn causes the controller to drop the data strobe line. After data strobe drops, the printer generates another character request when it is ready to accept another character. This sequence continues until the controller truncates the input by activating the control bit signal in response to the character request. The control bit (print direction function) is sent to end the data input and initiate a print cycle for that line of output.

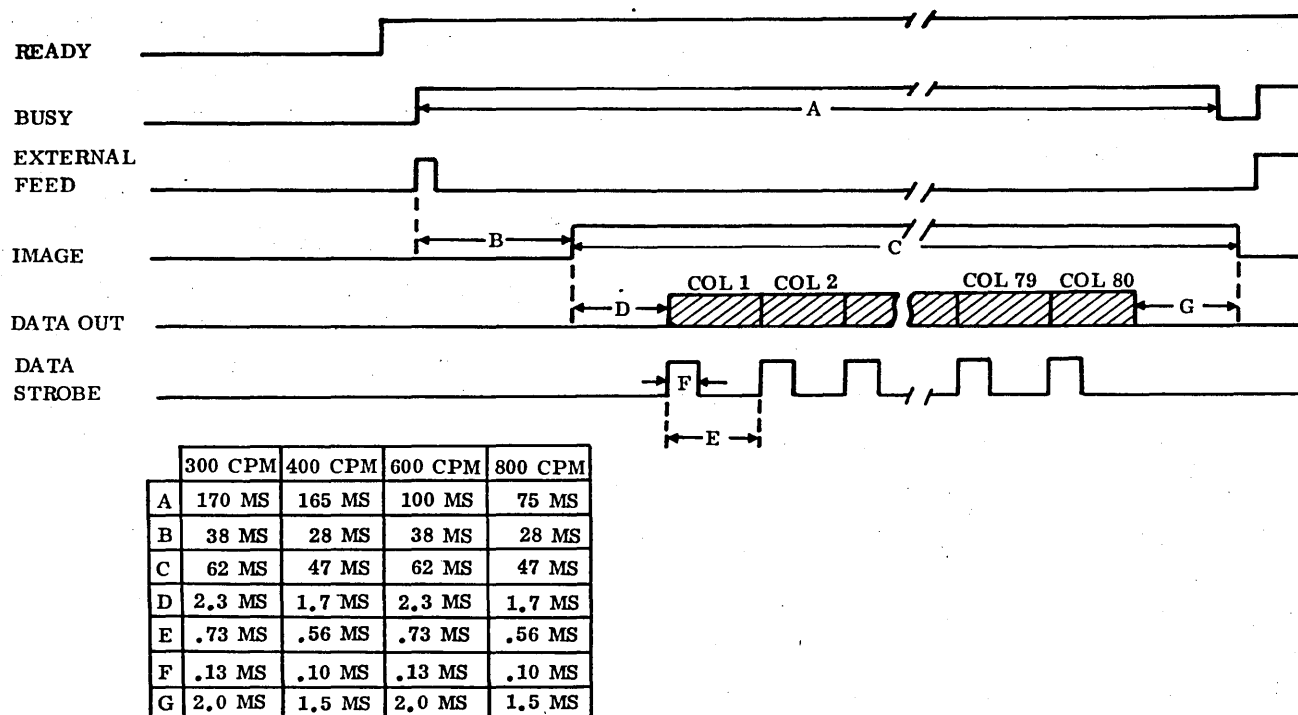
CARD READER CONTROLLER

During a CPU input/output operation, the equipment number contained in bits 7 through 10 of the address word is compared to the card reader controller's equipment number. When the controller is enabled and the address word equipment code matches the jumper selected card reader equipment number, address bits 0 and 1 combine with the read/write signal to determine the controller's operating mode. A description of the controller's operating modes is present in section 2.

The card reader controller can generate data, end of operation, alarm, common, and auto-data transfer interrupts. These five interrupts are brought to an interrupt selection matrix where any two of the

five can be jumpered to either of two CPU interrupt lines.

Basic card reader interface timing is shown in figure 4-5. A one-card read cycle is initiated by the controller activating the feed line to the card reader. The feed line may be activated by either the feed request director function or the manual feed switch. The controller activates the feed line only when the busy line from the card reader is inactive. Receipt of the feed signal raises the busy and image lines. As the leading edge of the card passes under the read station, a dynamic dark check (light is reflected for all rows) is performed to verify proper operation of the photo sensors. If the card reader fails to pass the dark check, the ready line drops and the read cycle is terminated. When no error occurs, the card reader sends a strobe signal to the controller when the data for card column 1 is valid. Approximately 720 microseconds later, a second strobe signal is generated to indicate that data for column 2 can be sampled. A total of 80 strobes occurs during each card cycle, regardless of the card data pattern. At the 81st column time, the card reader performs a late dark check. At column 89 time, the card reader drops the image line and performs a light check to verify proper photo sensor operation and card timing. If an error is detected, the card reader activates the read check signal. When the card reader is able to accept another feed command, it deactivates the busy signal.



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Figure 4-5. Basic Card Reader Input/Output Timing

CARD READER DEADSTART

A card reader deadstart operation is initiated by either a micro program within the micro-programmable processor or a remote pushbutton switch. In either case, the deadstart is initiated by the setting of processor status/mode bit 204 (SM204). The purpose of the deadstart operation is to allow the card reader to duplicate maintenance panel functions directly through the panel interface. If the processor is configured without a maintenance panel, the deadstart occurs through the I/O-TTY interface via the 1700 emulator's panel simulation capability. Regardless of the interface, the capabilities of the card reader deadstart operation are exactly the same as the capabilities offered by the maintenance panel or its simulation. Therefore, characters read from the card reader must conform to those characters used by the maintenance panel interface. Legal characters are numbers 0 through 9 and alphabetic characters A through M. Characters must be punched on the cards in the same sequence and fashion as if they were being entered on a remote teletypewriter through the panel interface or locally through the maintenance panel. Blank columns are allowed anywhere on the card since the card reader controller ignores blank columns during deadstart.

During card reader deadstart, cards punched with legal Hollerith characters are read at the maximum rate of the card reader, converted to ASCII code, and transmitted serially to the CPU. Timing for the deadstart operation is provided by a 153.6 kHz clock signal that is divided by 16 to produce the 9.6 kHz clock signal illustrated in figure 4-6.

Converted Hollerith data for a card column is transmitted to the panel interface or I/O-TTY interface in a serial stream consisting of a start bit, the seven-bit ASCII code, a parity bit, and one or more stop bits. Each 9.6 kHz clock pulse generates one bit of the serial data word to the processor. Therefore, at least 1040 micro-seconds (104 microseconds per bit times at least 10 bits) is required to transmit one ASCII character to the

panel interface. If the card reader being used reads cards faster than one column every 1040 microseconds, one or more columns must be left blank after each punched column. For example, the 300/600 cards-per-minute card reader reads a column every 720 microseconds, so one blank column must follow each punched column to provide the 1040 microsecond minimum time required to transmit the punched character to the CPU. If a card reader reads cards faster, more columns must be blank. The timing relationship of card columns read to serial data transmitted to the processor is shown in figure 4-7.

As a card passes through the card reader read station, column data (logical 1) is detected when a row hole causes no light to be reflected. A column strobe is generated for each card column and occurs approximately 20 microseconds after column data is detected.

During deadstart, the first column with holes punched becomes the first column converted to ASCII, loaded into the shift register, transmitted to the CPU. Columns without row pulses are detected as blank columns. A blank column prevents the shift register from loading the ASCII code.

As can be seen in figure 4-7, the start bit is transmitted to the panel interface when the shift register is loaded. The next clock pulse shifts the ASCII code in the shift register and bit 0 is transmitted. Each successive clock pulse shifts the character one place in the shift register and transmits the next bit to the processor. When the column strobe for column 2 occurs, no row hole punch is detected (assuming a card reader with data punched in column 1). The blank column prevents the shift register from being loaded. The shift register continues to be shifted every clock time. After all data and parity bits have been transmitted to the processor, stop bits are transmitted until the next column with row hole punches is converted to ASCII code and locked into the shift register.

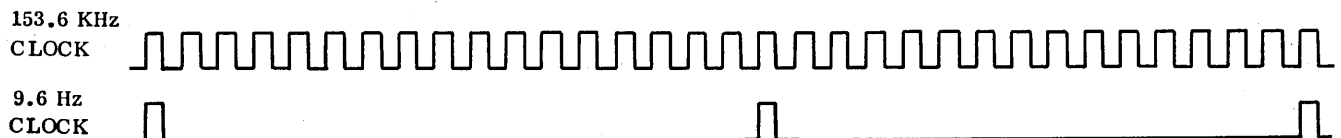


Figure 4-6. Deadstart Clock

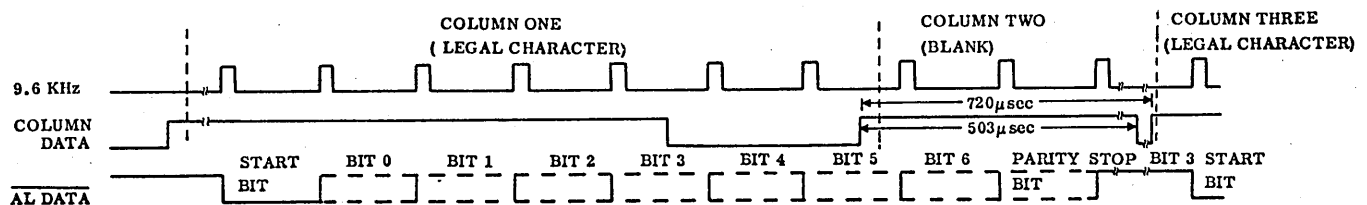


Figure 4-7. Deadstart Timing

TEST MODE

The line printer and card reader controllers are designed in such a way that each controller can be used to test the other. Together, the two controllers contain a program-controlled test mode that is activated by addressing the card reader controller. Test mode provides internal switching of data and control signals directly in front of the transmitter and receiver interfaces to the peripherals. During test mode operations, signals to and from the peripherals are disabled, so the I/O cables need not be removed.

With proper programming, all I/O signals and most internal controller functions and status can be tested independently of the end peripheral devices. A more detailed explanation of test mode sequences is presented in section 6.

INTERFACE SIGNALS

CPU INTERFACE SIGNALS

The card reader/line printer controller interfaces to the A/Q channel created by the I/O-TTY interface of the micro-programmable processor. The A/Q channel interface utilizes open collector TTL transmitter/receiver circuits. Table 4-2 lists the interface signals' controller pin assignments along with the signals' active level and direction of transmission.

CARD READER INTERFACE SIGNALS

The signal interface between the controller and the card reader is implemented using integrated circuit TTL transmitter and receivers. Table 4-3 defines the card reader interface signal pin assignments. Also shown in table 4-3 is the active level and direction of transmission of the interface signals. The following signals are transmitted between the card reader controller and the card reader.

External Feed

This signal is transmitted from the controller to indicate that the card reader should initiate a one-card read cycle.

Ready

The ready signal from the card reader indicates that the card reader is ready for operation. This signal is disabled by hopper empty, stacker full, read alert, jam, or logic power off condition.

Busy

When this interface line from the card reader is low, the card reader is on line and can accept a feed command. The busy signal goes high for any read alert or card alert condition, by de-activating the on-line switch or in response to a feed command.

Read Check

This interface line from the card reader indicates that a read alert or card alert condition has been detected. The read check signal occurs only during the card cycle on which the offending condition was detected and must be manually cleared.

Strobe

The card reader generates the strobe signal when data is stabilized on the data lines and is ready to be input by the controller.

Column Data

Data from the card reader is transmitted to the controller on 12 column data lines. A column data line is low (logical 1) when a punched hole is sensed in the corresponding row of the data card.

Image

This interface line from the card reader indicates that a card is in the read station. The image signal goes high when a card enters the read station and drops at the 89th column time.

Hopper Empty

The hopper empty line from the card reader indicates that the input hopper is empty and the last card has been read.

Stacker Full

The stacker full interface line from the card reader indicates that the output stacker is full and that the last card fed has been read.

Card Supply

This interface line from the card reader indicates that a hopper empty or stacker full condition exists.

Feed Error

The feed error line from the card reader goes low to indicate that the card reader was not able to feed the next card from the deck after two feed attempts.

Stack Error

A stack error from the card reader indicates a jam in the card path from the read station to the stacker.

Motion Error

This interface line from the card reader indicates that a feed error or stacker error condition exists.

TABLE 4-2. A/Q INTERFACE SIGNALS

Signal	Pin	Direction	Active Level	Function
RD01/	204	TO CPU	LOW	} LSB (A00) Data word (A) bits from the peripheral controller. In a read operation, the 16-bit data word is transferred from the controller to the computer.
RD02/	206	TO CPU	LOW	
RD03/	208	TO CPU	LOW	
RD04/	210	TO CPU	LOW	
RD05/	214	TO CPU	LOW	
RD06/	218	TO CPU	LOW	
RD07/	221	TO CPU	LOW	
RD08/	224	TO CPU	LOW	
RD09/	226	TO CPU	LOW	
RD10/	229	TO CPU	LOW	
RD11/	231	TO CPU	LOW	
RD12/	234	TO CPU	LOW	
RD13/	236	TO CPU	LOW	
RD14/	239	TO CPU	LOW	
RD15/	241	TO CPU	LOW	
RD16/	244	TO CPU	LOW	
SD01/	203	FROM CPU	LOW	} MSB (A15) } LSB (A00) Data word (A) bits to the peripheral controller. In a write operation, the 16-bit word is transferred from the computer to the controller.
SD02/	205	FROM CPU	LOW	
SD03/	207	FROM CPU	LOW	
SD04/	209	FROM CPU	LOW	
SD05/	211	FROM CPU	LOW	
SD06/	215	FROM CPU	LOW	
SD07/	219	FROM CPU	LOW	
SD08/	223	FROM CPU	LOW	
SD09/	225	FROM CPU	LOW	
SD10/	228	FROM CPU	LOW	
SD11/	230	FROM CPU	LOW	
SD12/	233	FROM CPU	LOW	
SD13/	235	FROM CPU	LOW	
SD14/	238	FROM CPU	LOW	
SD15/	240	FROM CPU	LOW	
SD16/	243	FROM CPU	LOW	

TABLE 4-2. A/O INTERFACE SIGNALS (Contd)

Signal	Pin	Direction	Active Level	Function
ADR01/	280	FROM CPU	LOW	LSB (Q00) Address (Q) bits to the peripheral controller. The nine highest order bits uniquely specify the device. The lower seven bits specify functions. MSB (Q15)
ADR02/	247	FROM CPU	LOW	
ADR03/	246	FROM CPU	LOW	
ADR04/	245	FROM CPU	LOW	
ADR05/	212	FROM CPU	LOW	
ADR06/	217	FROM CPU	LOW	
ADR07/	222	FROM CPU	LOW	
ADR08/	281	FROM CPU	LOW	
ADR09/	282	FROM CPU	LOW	
ADR10/	283	FROM CPU	LOW	
ADR11/	284	FROM CPU	LOW	
ADR12/	285	FROM CPU	LOW	
ADR13/	286	FROM CPU	LOW	
ADR14/	287	FROM CPU	LOW	
ADR15/	288	FROM CPU	LOW	
ADR16/	289	FROM CPU	LOW	
READ-SSTB/	248	FROM CPU	LOW	Initiates an input transfer of one data word. (READ)
WRITE/	290	FROM CPU	LOW	Initiates an output transfer of one data word.
REPLY/	216	TO CPU	LOW	Indicates controller acceptance of a computer read or write. The reply drops after the read or write drops.
REJECT/	220	TO CPU	LOW	Indicates controller response to a computer read or write when the operation cannot be performed.
MR/	46	FROM CPU	LOW	Clears the peripheral controller and the external equipment. (MASTER CLEAR)
PROG-PROT/	291	FROM CPU	LOW	Indicates that this data transfer was initiated by an I/O instruction whose program protect bit is set.
WEO/	292	TO CPU	LOW	Indicates that bits 11, 12, 13, 14, and 15 of the address are all zero. (W=0)
RDINTxx/	250	TO CPU	LOW	Interrupt line - micro
RPINTxx/	249	TO CPU	LOW	Interrupt line - macro
RDINTxx/	50	TO CPU	LOW	Interrupt line - micro
RPINTxx/	49	TO CPU	LOW	Interrupt line - macro

TABLE 4-3. CARD READER INTERFACE SIGNALS

Signal	Controller Backplane Pin No. Signal	Reader Connector Pin No. Signal/Return	Direction	Active Level
EXTERNAL FEED/	99	C/H	TO READER	LOW
READY	90	n/t	FROM READER	HIGH
BUSY	94	A/E	FROM READER	HIGH
READ CHECK/	98	D/J	FROM READER	LOW
STROBE/	293	B/F	FROM READER	LOW
IMAGE/	93	M/S	FROM READER	LOW
DATA ROW 0/	83	f/m	FROM READER	LOW
DATA ROW 1/	279	K/P	FROM READER	LOW
DATA ROW 2/	86	N/T	FROM READER	LOW
DATA ROW 3/	79	L/R	FROM READER	LOW
DATA ROW 4/	82	W/a	FROM READER	LOW
DATA ROW 5/	87	U/Y	FROM READER	LOW
DATA ROW 6/	81	X/b	FROM READER	LOW
DATA ROW 7/	85	V/Z	FROM READER	LOW
DATA ROW 8/	84	e/k	FROM READER	LOW
DATA ROW 9/	80	e/h	FROM READER	LOW
DATA ROW 11/	88	d/j	FROM READER	LOW
DATA ROW 12/	89	r/v	FROM READER	LOW
HOPPER EMPTY/	91	x/w	FROM READER	LOW
STACKER FULL/	95	y/w	FROM READER	LOW
CARD SUPPLY/	294	z/w	FROM READER	LOW
FEED ERROR/	96	AA/DD	FROM READER	LOW
STACK ERROR/	92	BB/DD	FROM READER	LOW
MOTION ERROR/	97	CC/DD	FROM READER	LOW
GROUND	78, 278, 102, 302			

LINE PRINTER INTERFACE SIGNALS

The signal interface between the controller and the line printer is implemented using integrated circuit voltage-mode differential transmitters and receivers. Table 4-4 defines the line printer interface signal pin assignments. The printer interface provides both high true and low true interface signals. The following signals are transmitted between the controller and the line printer.

Ready

The ready signal is transmitted from the line printer when the printer is fully operational. This signal indicates that no alarm conditions exist and the control panel start button has been depressed.

Line Ready

This interface line from the line printer indicates that the printer is ready to accept a line of data. The line ready interface line becomes true preceding the generation of the first character request and remains true until the control bit (print command) is received. This line remains false during a print cycle, thereby indicating that the printer cannot accept data.

Character Request

The character request interface line from the line printer indicates that the printer is ready to accept a data character from the controller. The controller must sense this signal before it can send a data strobe signal. This interface line goes false after the data byte has been sampled, and goes true when the printer can accept another character.

Data Strobe

This interface line from the controller indicates to the printer that the data lines are established and the data byte can be sampled.

Data Bits

Eight data lines carry the control codes and data characters from the controller to the line printer.

Control Bit

The control bit interface line from the controller indicates to the printer that the data input is being truncated, and commands the printer to begin a print cycle.

Parity Bit

The parity bit line from the controller indicates the parity of the data currently on the data lines. Odd or even parity is determined by the position of the parity jumper within the card reader controller.

Master Clear

This signal from the controller indicates to the printer that all circuits should be placed in their initial condition.

Load Image Request

This interface signal is used only by printers that contain image memory. The load image request line from the printer indicates that the printer places the next 288 data characters in its image memory. The codes in the image memory represent the codes for the characters in the type array. This signal must be initiated manually from the printer.

Error

The error interface line from the printer indicates that the printer has detected an error condition. Various printers that can be used with the card read/line printer controller have different error conditions; therefore, refer to the specific line printer's maintenance manual for more detailed information. The error signal is removed by a buffer clear or master clear signal from the controller.

Buffer Clear

This interface signal from the controller clears printer error conditions without disturbing any other printer operation. The buffer clear signal conditions the printer for a new line of data. Buffer clear is a 5-microsecond pulse.

Paper Out

This optional status line from the printer indicates an out-of-paper condition exists at the lower tractor switches.

Buffer Overflow

This optional interface line from the printer indicates that more than the maximum number of characters (per line) has been received. The buffer overflow line becomes true during transfer of the first extra data byte and is cleared when a control bit signal truncates the input.

TABLE 4-4. LINE PRINTER INTERFACE SIGNALS

Signal	Controller Backplane Pin No.†	Printer Connector Pin No.†	Direction
DATA STROBE	258/253	B/A	TO PRINTER
CHARACTER REQUEST	259/58	D/C	TO PRINTER
DATA BIT 0	66/68	E/F	TO PRINTER
DATA BIT 1	64/62	H/J	TO PRINTER
DATA BIT 2	273/275	K/L	TO PRINTER
DATA BIT 3	63/262	M/N	TO PRINTER
DATA BIT 4	69/269	P/R	TO PRINTER
DATA BIT 5	61/263	S/T	TO PRINTER
DATA BIT 6	270/70	U/V	TO PRINTER
DATA BIT 7	267/67	W/X	TO PRINTER
NOT USED		Y/Z	
CONTROL BIT	255/252	a/b	TO PRINTER
PARITY BIT	274/276	c/d	TO PRINTER
BUFFER CLEAR	254/256	f/e	TO PRINTER
READY	56/59	j/h	FROM PRINTER
LINE READY	53/55	m/k	FROM PRINTER
MASTER CLEAR	54/257	p/n	TO PRINTER
PAPER OUT	265/65	s/r	FROM PRINTER
BUFFER OVERFLOW	260/261	u/t	FROM PRINTER
ERROR	60/57	w/v	FROM PRINTER
GROUND	76	x	GROUND
LOAD IMAGE REQUEST	264/266	AA/Z	FROM PRINTER
†The first signal pin of the two shown in the high true positive level for the related interface signal. The second pin number is low true for the same interface signal.			

This section presents a functional description of the logic diagram at the back of this section.

BOARD DESCRIPTION

The card reader/line printer controller is constructed utilizing transistor-to-transistor logic (TTL) integrated circuit concepts with both small-scale integration (SSI) and medium-scale integration (MSI) circuits. The integrated circuits are mounted on one 11- by 14-inch

three-layer printed circuit board. Each integrated circuit's position on the board is identified by the alphanumeric matrix shown in figure 5-1. The printed circuit board is inserted into a card slot of the CPU's chassis that is connected to the backplane via a double row of 102 input/output pins. The pins are labeled 1 through 102 and 201 through 302. Two cable connectors slip over the input/output pins of the controller's board slot on the CPU chassis backplane to connect the controller to the line printer and the card reader. The line printer connects to pins 52 through 76 and 252 through 276 while the card reader connects to pins 78 through 102 and 278 through 302.

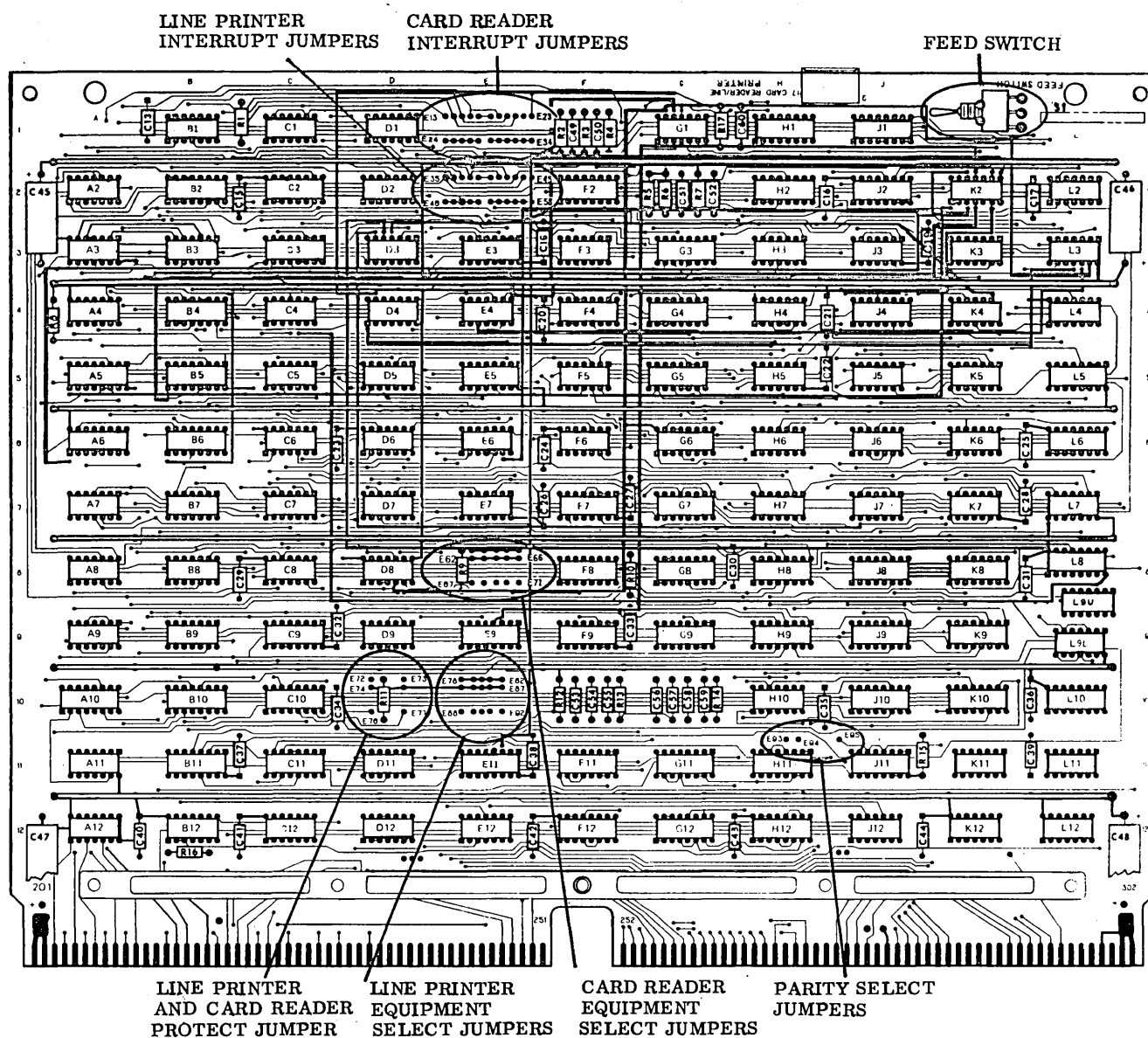


Figure 5-1. Controller 88909503 Integrated Circuit Placement

KEY TO LOGIC

Each logic diagram is divided into an alphanumeric grid. The vertical axis is labeled A through D and the horizontal axis is labeled 1 through 8. The first two logic diagram sheets show the input/output signal pin assignments along with the page and alphanumeric coordinate where the signal appears on the diagrams.

Signal names shown on the logic diagrams provide a means of tracing signals from one diagram to another. Input/output signals are shown on the diagrams by an input or output pin symbol with the pin number written above it. A square with a number in it indicates that a signal is used on another page of the diagrams. The number within the square specifies the origin or destination of the signal. Most logic signals to and from the card reader/line printer controller are low true, meaning that the logical 1 signal level is a TTL low ($0.5v \pm 0.5v$). These low true, external signals are indicated with a slash (/) following the mnemonic. These mnemonics identically match those found in the wire list of the processor.

Signals internal to the CR/LP controller that are low true are shown with a bar (xxx̄) over the signal mnemonic. Signal mnemonics with neither a slash nor a bar are high true signals (i.e., logical 1 = $4.5v \pm 0.5v$). Each logic symbol on the diagrams contains an alphanumeric locator that shows the board coordinates where the integrated circuit is located on the controller circuit board. This alphanumeric locator is used in the diagram descriptions to locate specific components on the printed circuit board.

The five-digit number shown within or adjacent to each logic symbol is a reference part number for the integrated circuit. This number provides a way of locating the integrated circuit's operating characteristics by referencing the logic element number to the generic integrated circuit part number in table 5-1.

Use this generic number to obtain the integrated circuit description from the manufacturer's data book.

TABLE 5-1. CARD READER/LINE PRINTER INTEGRATED CIRCUITS

Logic Element Number	Description	Generic Number
67601	Synchronous 6-bit binary rate multiplexer	7497
67605	4-bit magnitude comparator	7485
72601	Quad 2-input NAND	74H08
72801	Dual 2-to-4 line decoder	74150
72901	4-bit bidirectional shift register	74194
73601	Quad 2-input NAND	74H00
74002	Quad D-type flip flop, clear	74175
74201	Triple 3-input NAND	74H10
75701	Hex buffer, high voltage, OC	7407
75901	Dual 4-input multiplexer	9309
76001	Dual differential line receiver	9615
76101	Differential line driver 3-state	8831
95401	J-K flip-flop	74109
96201	Quad 2-input NOR	7402
96301	Quad 2-input buffer NAND	7437
96405	Quad exclusive OR	9014
97701	Parity generator	74180
98001	Quad 2-input multiplexer	74157, 9322
98101	Dual one-shot	9602
99601	Hex inverter	74H04

LOGIC DIAGRAMS

The logic diagram descriptions are applicable to the functional block diagram figure 5-2 of the card reader/line printer controller. The numbers boxed in the upper right corners of the blocks indicate the sheet of the logic diagram where that particular function can be found.

The logic diagram is applicable to PWA 88909502 and PWA 88909503. Sheet 17 of the logic diagram figure illustrates the wiring and component differences between the two PWAs. This sheet shows the additions to the 88909502, in dotted lines, that created the 88909503 PWA.

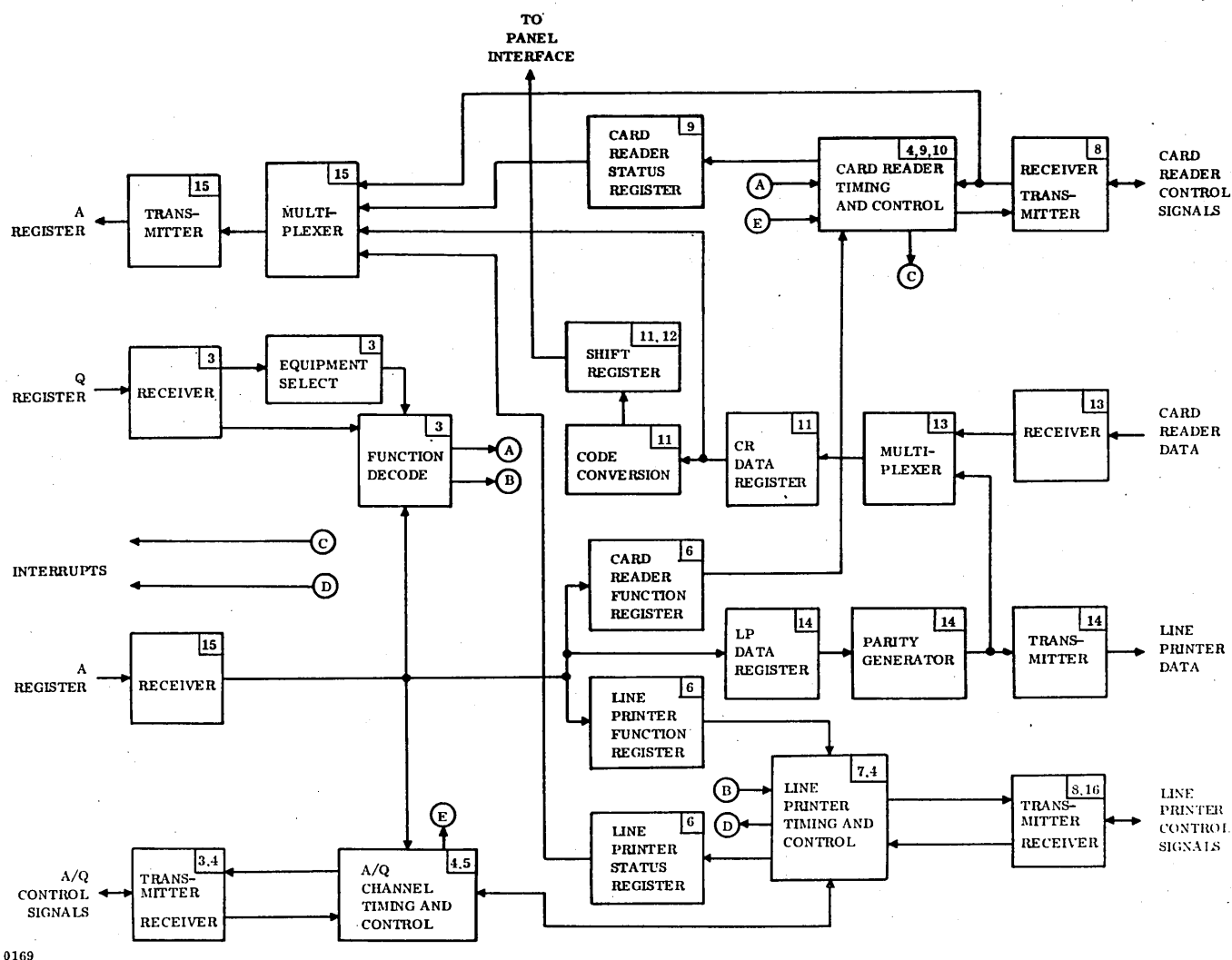
EQUIPMENT SELECT AND FUNCTION CODE

Address bits 7 through 10 (ADR8 thru ADR11) provide the equipment number portion of the address. These bits are compared to the equipment number selected by the equipment select jumpers. Pin 6 of the

compare chip at E9 or E11 is a logical 1 when the equipment number portion of the address matches the equipment number selected by the jumpers. The equipment number jumpers connected to E11 pins 10, 12, 13, and 15 select the line printer equipment number. A ground represents a logical 0, and the +5v (RES COM 1) line represents a logical 1. The logic diagram shows equipment number C₁₆ selected for the line printer. The card reader equipment number is selected by the jumpers connected to E9 pins 10, 12, 13, and 15. Equipment number 1₁₆ is shown selected for the card reader.

The jumpers connected to D8 pin 8 and E6 pin 6 are equipment enable/disable jumpers. When an enable/disable jumper is in the disable position, the corresponding controller's compare chip output is disabled.

WEO indicates that address bits 11 through 15 (ADR12 through ADR16) are all zeros. When address bits 11 through 15 are all zero and the equipment is enabled, the compare chips generate (CR+CL)(R+W) to the interrupt select and reply or reject logic.



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Figure 5-2. Card Reader/Line Printer Controller Block Diagram

During test mode, the disabled controller is addressed by using address bit 6 (ADR07/) via the inverter (D12 pin 4) and the enabled controller's equipment number compare to generate (CR+LP)(R+W).

Address bits 0 and 1 (ARD01/ and ADR02/) are decoded by the demultiplexer chip at E5 to select a controller operation. For example, LPX0 (P4-6) goes low when the line printer is addressed and address bit 0 (ARD01/) is set. As another example, CR11 goes low (E5 pin 12) when the card reader is addressed and address bits 0 (ADR01/) and 1 (ADR02/) are set. This corresponds to the card reader director status operation.

Logic signals SELA and SELB (E4 pins 8 and 3) represent the encoding of both card reader and line printer input operations. These terms drive the selection control inputs of the A register interface multiplexer. Following this selection, the appropriate data is gated to the read data (RDxx) lines.

INTERRUPT SELECT AND REPLY OR REJECT

The jumpers shown connected to inverters E12 pins 5, 9, 11, and 13 that drive the RINTx, RPINT, and RDINT backplane lines select the conditions that generate the two interrupts for each controller. Jumpers connected to E12 pins 9 and 11 select line printer interrupts, and the jumpers connected to E12 pins 5 and 13 select card reader interrupts.

The REPLY or REJECT signals to the CPU are generated by the one-shots at F2 and the flip-flops at E3. The positive-going leading edge of (CR+LP)(R+W) triggers the 280 nanosecond one-shot at F2 pin 6. The negative-going trailing edge of the F1 output pulse then triggers the 500 nanosecond (signal F2) one-shot. When signal F2 is triggered, the positive-going leading edge of the F2 output pulse sets or clears the reply flip-flop as determined by the REPLY COND signal. The response enable flip-flop at E3 sets on the negative-going trailing edge of the F2 output pulse. A reply or reject response to the CPU is generated by the output from the response enable flip-flop. The 280 nanosecond F1 time allows for internal function decode and setting of the REPLY COND signal. If REPLY COND is low at the leading edge of the F1 pulse, the reply flip-flop will not set. A reject signal is returned to the processor when the response enable flip-flop becomes set. The CR/LP controller generates a reply to the processor when the internal REPLY COND signal is set during the F1 pulse time. Figure 5-3 shows the timing relationship of the reply or reject circuitry.

The card reader and line printer program protect jumpers (figure 5-4) are connected to D9 pins 9 and 13. When a jumper is connected to the ground terminal, the controller is in the unprotected mode, and when the connection is to +5v, the controller is program protected. The line printer jumper is connected to D9 pin 9, and the card reader jumper is connected to D9 pin 13.

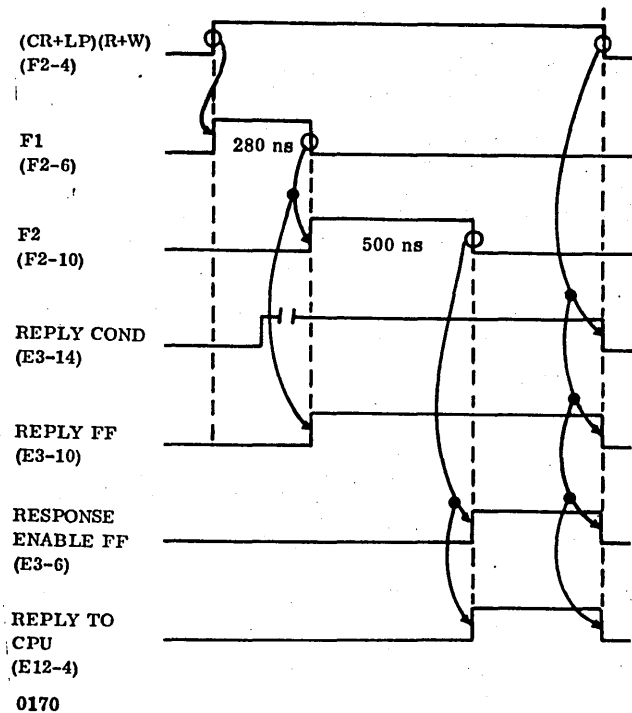


Figure 5-3. Reply or Reject Timing

FUNCTION DECODE AND REPLY ENABLE

The REPLY COND signal is set when a line printer data, card reader data, line printer function, card reader function, line printer status, card reader status 1, card reader status 2, or test mode operation is accepted. Table 5-2 shows the conditions that must exist before the operations are accepted. The letters preceding the operation names in the table are reference symbols on the diagrams where the condition is sensed.

INTERRUPT ENABLE REGISTERS

An interrupt is enabled or disabled by a director function operation. There is a separate flip-flop for each of the four interrupts (data, EOP, alarm, and ADT) for both the card reader and the line printer. The flip-flops are clocked at time F2. The F2 signal is ANDed with the LPFNCT or CRFNCT signals that are generated as a reply condition.

Line printer interrupt enables can also be cleared by the CLRPI signal. This signal is the logical OR of a clear controller or clear interrupt function. Likewise, card reader interrupt enables can also be cleared by the CLRCI signal.

The card reader ADT interrupt flip-flop (B4) is set as a result of the enabled interrupt (B5 pin 10) ANDing with the false condition of both the card reader alarm (A3 pin 11) and the card reader EOP interrupt (A4 pin 4).

TABLE 5-2. REPLY ENABLE CONDITIONS

Operation	Conditions
C Line printer function	(LPX1) ● WRITE ● LPPROTOK ● (A05 + LDSTAT ● LPRDY ● LPBSY)
G Card reader function	(CRO1) ● WRITE ● CRPROTOK ● (CRRDY + A02 ● A03 ● A04 ● A06 ● A07
B Line Printer data	(LPX0) ● WRITE ● LPRDY ● LPBSY ● LDSTAT ● LPPROTOK ●
E Card reader data	(CRO0) ● READ ● CRPROTOK ● CRALM ● CDSTAT
D Line printer status	(LPX1) ● READ
F Card reader status 1	(CRO1) ● READ
H Card reader status 2	(CRI1) ● READ
A Test mode	(CR10 ● WRITE ● CRPROTOK ● (LPBSY ● CRBSY + A00)

The line printer ADT interrupt flip-flop is enabled in the same way. However, the flip-flop clock term on B4 pin 4 is driven by the output of the 75 micro-second one-shot circuit at H1 pin 7. The one-shot is in turn triggered by the line printer character request (CHARREQ*) signal. The one-shot delays the maximum rate at which the line printer ADT interrupts can be generated so that the processor is not monopolized by virtually constant ADT interrupts.

The card reader ADT interrupt flip-flop is clocked with the load card reader data (LDCRD) signal directly, since the maximum rate of the card reader is not capable of causing constant ADT interrupts.

When an interrupt condition occurs, the interrupt is sent to the interrupt select logic where, if jumper-selected, it is sent to the CPU.

LINE PRINTER CONTROL

The multiplexer chips at F7 and G7 select signals from the line printer during normal mode and from the card reader controller during test mode. The I₀ inputs are selected on the multiplexer chips during test mode and the I₁ inputs are selected during normal mode. In addition to selecting the operation control signals for the line printer controller, the multiplexer outputs equipment status to the CPU.

The control bit flip-flop at G5 generates signal TMCS when a print command is issued to the printer (director function and A bit 05). The control bit flip-flop is clocked at F2 time during the A/Q command execution.

The line printer strobe flip-flop at G5 is set by each character output to the printer and by a print command. The line printer strobe flip-flop is also clocked at F2 time of the A/Q command execution. Data characters from the CPU lines are strobed into the characters data holding register by the LDLPD signal.

Note that both the control bit flip-flop and the line printer strobe flip-flop are set by the ENDLPADT signal. ENDLPADT causes the line printer controller to automatically initiate (as seen from a macro level) a line printer print cycle at the end of a line printer ADT output operation.

Also included on this logic page is the combination of logic that decodes the line printer's clear controller and clear interrupts director functions. The line printer EOP interrupt flip-flop F4 is set by the leading edge of the line printer line ready signal when the EOP interrupt is enabled (LPEOPRQ = 1). The line ready signal goes false at the beginning of a print cycle and goes true again when the print cycle is completed.

TRANSMITTERS AND RECEIVERS

During normal mode, the multiplexer chip at L10 selects status signals from the card reader. The strobe signal (STBF) from the line printer controller is selected to simulate the status signals during test mode.

The one-shot circuit at G3 generates the 5 microsecond buffer clear (LPCLR) pulse to the printer. The one-shot is triggered by the CLRFNCT signal as a result of a clear controller director function with A00 = 1. Additional logic shown here decodes the card reader clear controller and clear interrupts director functions. A logical OR of the card reader feed director function (CRF2 and bit 7) and the FORCE FEED signal is performed by the logic shown at the lower center of the sheet. Also shown here is the receiver circuit for the CPU master reset (MR) signal and the associated driver circuits. The driver circuits at H4 permit a large fan-out of the MCF signal.

The terminate ADT flip-flop at H2 becomes set when the line printer is addressed (LP) and the CPU generates the STERM/ signal. STERM/ is generated by the CPU coincident with the last data character output of an ADT buffer. The terminate ADT flip-flop enables the end LP ADT flip-flop at H2 to be set by the next printer character request (CHARREQ*) signal. The end line printer ADT flip-flop forces a print cycle via the control bit and line printer strobe flip-flops (G5). Both the terminate ADT and the end line printer ADT flip-flops are cleared by the clear ADT (CLADT) signal.

CARD READER CONTROL

Flip-flops B2, C2, C3 and F4 are card reader control flip-flops. The card reader EOP status flip-flop at C2 is set by the trailing edge of the card reader image CRIMAGE signal. The feed request flip-flop at C3 is set by the SETFEED signal and cleared by the trailing edge of the card reader clear feed (CLRFEED) director function or MCF signal.

When the interrupt is enabled (CREOPRQ = 1), the card reader EOP interrupt flip-flop at G6 is set by the same clock signal that sets the card reader EOP status flip-flop (C2). The card reader data flip-flop at B2 is set by the trailing edge of the card reader data strobe (CRSTB) signal if a lost data condition does not exist. The card reader data flip-flop is cleared by the ALCLR signal (via AND C6 pin 8) during a deadstart operation, by the CLDTA signal when the CPU reads card reader data, or by the fact that a new feed command has been issued (inverter F4 pin 2).

Normally, the SETFEED signal sets the card reader feed flip-flop at F4 and the feed request flip-flop (C3) at the same time. The output of the card reader feed flip-flop is gated (through L2 and L3) when the busy (BZY) signal is false and the normal mode (NM) signal is active high to generate the external feed (EXT FEED/) signal to the card reader. The card reader feed flip-flop is cleared by the image (CRIMAGE) signal or a clear controller (CLRC) signal.

Note that the card reader feed flip-flop is also set with the logical AND of the feed request flip-flop and the lockout flip-flop at C3.

If the CPU issues a feed command while the card reader controller is busy during a card cycle, the controller ignores all remaining data on the card currently being read. Neither a data status interrupt nor an EOP status interrupt is generated for the card. Upon receipt of the feed command, the controller generates a feed signal and resumes reading data from column 1 of the next card. The controller does this by clearing the valid card flip-flop (C2) and setting the lockout flip-flop (C3) when the feed function (FEEDFNCT) signal is issued while the controller is busy (CRBSY). When the valid card flip-flop is clear, it inhibits the CRSTB signal that prevents the card reader data flip-flop from setting. When the lockout flip-flop is set, it prevents CRIMAGE signal from setting the card reader EOP status and EOP interrupt flip-flops and from clearing the feed request flip-flop.

The valid card flip-flop is again set by the not busy (RDYNBZY) signal at the end of the first card. This in turn allows the data strobe (CRSTB) signal from column 1 of the next card to clear the lockout flip-flop. Since the feed request flip-flop was not allowed to clear at the trailing edge of the first card (normally via CRIMAGE), the card reader feed flip-flop sets and causes the next card to be fed.

Following the first data strobe of this next card, input data is processed normally through to the EOP

unless the CPU again issues another feed command prior to the completion of this card.

The card reader lost data flip-flop at B2 pin 6 set when a data strobe (CRSTB) signal is received and the CPU has not yet read the previous data column (the card reader data flip-flop is still set).

CARD READER CONTROL SIGNAL RECEIVER

The multiplexer chip at L8 selects the card reader interface signals during normal mode. During test mode, the multiplexer selects the interface line printer control signals instead of the card reader interface signals.

The combinational logic produced by J7 and K7 creates the card reader ready (CRRDY) condition. A lost data condition (LOSTDTA = 0) or the card reader not ready condition (CRRDY = 0) creates the card reader alarm (CRALM) condition (E7).

The cross-coupled inverters at B12 serve as a switch debounce circuit. The output of the inverter at H6 pin 8 SET SM204/) causes the deadstart status/mode flip-flop in the processor to set. Note that the system deadstart switch may or may not be wired to this debounce circuit. Other debounce circuits are provided elsewhere in most systems (i.e., other peripheral controllers or the I/O-TTY interface).

CARD READER DEADSTART

The card reader deadstart logic receives parallel Hollerith card reader data, converts it to ASCII code, and transmits the ASCII codes serially to the CPU.

Table 5-3 shows the Hollerith-to-ASCII conversion equations.

TABLE 5-3. HOLLERITH-TO-ASCII CONVERSION EQUATIONS

ASCII Bit	Shift Reg. Input Pin	Punched Holes by Row Number
(LSB) 0	J2 pin 5	11 (1+3+7+9)+11 (2+4+6)
1	J2 pin 4	2+6+11 (3+7)+11 (1+5)
2	J2 pin 3	11 (4+5+6+7)+11 (1+2)
3	J1 pin 6	11 (8+9)+11
4	J1 pin 5	11 • 12
5	J1 pin 4	11 • 12
(MSB) 6	J1 pin 6	11 + 12

When card reader row data is input, the circuitry in the center of the page checks for a blank column (K5 pin 8). Hollerith data is converted to ASCII codes, and the exclusive OR gates generate even parity (L3 pin 6). The serial shift registers at J1 and J2 are loaded with a start bit and an ASCII character code. The ground input pin 6 of J2 is transmitted as the start bit to the CPU when the shift register is parallel-loaded with the ASCII code. The 9.6 kHz clock input shifts data within the serial shift register every 104 microseconds. After each shift, the next higher data bit is transmitted to the CPU on backplane output pin 41. The output (PARITYFF) of the parity flip-flop (L5) is the serial input to the shift register at J1 when the first shift occurs; then the parity flip-flop is cleared. The second shift clocks the cleared output of the parity flip-flop into the shift register at J1. The cleared output of the parity flip-flop is eventually shifted down and transmitted to the CPU as the stop bit. Approximately 1.0 millisecond is required to load the data and shift it out to the CPU during a card reader deadstart (10 bits at 104 microseconds per bit). When a card reader reads cards faster than one column every 1.0 millisecond, blank columns must be inserted between the punched columns. For example, the 300/600 cards per minute card reader reads a card column every 0.72 milliseconds. Therefore, every second column must be blank to provide the 1.0 millisecond (or more) required by the controller to complete the deadstart serial data transfer. The blank column (BLANK) signal inhibits the loading of the serial shift registers. The serial shift registers continue to shift every 104 microseconds regardless of whether data is in the register or not. Consequently, stop bits are continually transmitted to the CPU until another card column is read and loaded into the shift registers.

The 9.6 kHz clock that provides control for the deadstart operation is derived from a 153.6 kHz clock (DSUARTCLK) provided by the CPU. This conversion is accomplished by the binary rate multiplexer L6.

The binary rate multiplier chip at L6 divides the deadstart clock rate (normally 153.6 kHz) input by 16 to produce the deadstart control clock (normally 9.6 kHz). The 9.6 kHz clock is a 3.24 microsecond wide positive pulse that occurs every 104 microseconds at L6 pin 5).

A deadstart operation is inhibited when the processor sets the status mode bit 204 (SM204/ goes low). If the card reader is ready, the FORCE FEED signal causes a card cycle to be initiated.

When a card reader column is read by the card reader and data is loaded into the holding register, the card reader data status flip-flop is set. The leading edge of the next clock pulse sets

the load flip-flop and clocks parity into the parity flip-flop (L5 pin 6). The Hollerith data is converted to ASCII and, if the card column being read is not blank, the ASCII character is loaded into the serial shift register.

ALCLR is generated by the trailing edge of the positive clock pulse and clears the data status flip-flop. The leading edge of the next clock pulse clears the load flip-flop. Subsequent clock pulses shift the data out serially. This sequence continues, one card column at a time, until the SM204/ signal goes high. The cross-coupled gates at J7 allow the deadstart to continue through the end of the card in process (until BZY goes low).

The feed switch connected to NOR K4 pin 8 forces the card reader to feed cards until the switch is turned off.

CARD READER INPUT DATA

During normal operation, the multiplexer chips at K8, and K10 select input data from the card reader by way of the I_0 input pins. Output data for the line printer controller is selected through the multiplexer (I_1 input pins) during test mode. Actual or simulated card reader row data is stored in the flip-flop registers at J8, J9, and J10 and is transmitted to the CPU by the CPU data transmitters. This 12-bit holding register is loaded by the LDCRD signal.

Data received from the card reader is driven by open collector TTL circuits. Each signal is terminated within the CR/LP controller with a resistor network at integrated circuit locations K11 and K12.

LINE PRINTER OUTPUT DATA

CPU A register output data from the CPU data receivers is gated into the flip-flops at H8 and H9 by the load line printer data term (LDLPD). The complemented output of the data flip-flops is used by the chip at H10 to generate parity. The pin 5 output generates even parity while the pin 6 output is used for odd parity. During normal mode, the data flip-flop's complemented output and the parity bit are transmitted to the line printer when the data flip-flops are loaded. When test mode is selected, the data and parity bits are gated into the multiplexer chips at K8, K9, and K10 as input data.

The line printer transmitter data circuits are shown at integrated circuits G11, H11, J11, G12, and H12. The transmission scheme utilized is differential voltage mode that exhibits exceptional signal transmission characteristics when used with twisted pair cables and differential receivers.

CPU DATA TRANSMITTERS AND RECEIVERS

TABLE 5-4. INPUT DATA SELECTION

The transmitters transmit data bits 0 through 11 (terms RD01/ through RD12/) to the CPU's A register. Data bits 12 through 15 are not used by the card reader/line printer controller.

The CPU's A register input data word from the CR/LP controller may contain card reader status, line printer status, or card reader input data. The multiplexer control inputs select the data passed through the transmitters and are shown in table 5-4.

Also shown on this diagram are the CPU data receivers for bits 0 through 7 (SD01/ through SD08/). Output data bits 8 through 15 are not used by the CR/LP controller.

Operation	Read	SELB	SELA	Input Selected
CR status 2	1	0	0	D ₀
CR status 1	1	1	0	D ₁
CR data	1	0	1	D ₂
LP status	1	1	1	D ₃

Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 1 of 1/)

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MCA-DPD FORM NO. E-1265

Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 2 of 17)

DETACHED REVISIONS
 96744220 A
 315-053-6161



(25,4000)
1 INCH

96744220 A
 315-053-6161

FUNCTION	INPUT PIN	OUTPUT PIN	PAGE/ZONE	REMARKS
IMAGE/	93		10-D8	
LINEREADY	55		16-B8	
LINEREADY/	53		16-B8	
LOADIMAGE	266		16-D4	
LOADIMAGE/	264		16-D4	
MASTERCLR		54	8-B4	
MASTERCLR/		257	8-B4	
MCF		3	8-B4	
MOTIONERR/	97		10-C8	
MR/	46		8-A6	
PAPEROUT	65		16-C4	
PAPEROUT/	265		16-C4	
PARITYBIT		274	14-D1	
PARITYBIT/		276	14-D1	
PROG-PROT/	291		4-A7	

FUNCTION	INPUT PIN	OUTPUT PIN	PAGE/ZONE	REMARKS
RD01/		204	15-D6	
RD02/		206	15-C6	
RD03/		208	15-C6	
RD04/		210	15-B6	
RD05/		214	15-A6	
RD06/		218	15-A6	
RD07/		221	15-D3	
RD08/		224	15-C3	
RD09/		226	15-C3	
RD10/		229	15-B3	
RD11/		231	15-A3	
RD12/		234	15-A3	
RDINTXX/		250	4-B6	LP MICRO
RDINTXX/		58	4-B2	CR MICRO
READCHECK/	98		10-B8	
READ-SSTB/	248		3-D4	
READY	59		10-B8	
READY/	56		16-B8	
READY*	90		10-B6	
REJECT/		220	4-C1	
REPLY/		216	4-C1	
RPINTXX/		249	4-B6	LP MACRO
RPINTXX/		49	4-B2	CR MACRO
SD01/	203		15-D2	
SD02/	205		15-D2	

FUNCTION	INPUT PIN	OUTPUT PIN	PAGE/ZONE	REMARKS
SD03/	207		15-D2	
SD04/	209		15-C2	
SD05/	211		15-C2	
SD06/	215		15-C2	
SD07/	219		15-C2	
SD08/	223		15-B2	
SETSM204/		21	10-A5	CUSTOM WIRED
SM204/	44		12-B7	
STACKERR/	92		8-D3	
STACKFULL/	95		8-D3	
STERM/	48		8-C8	
STROBE/	293		10-D8	
SWNC	16		10-A7	
SWNO	20		10-A7	
TERM 1	36		15-B3	UNDEFINED
TERM 2	37		15-B3	UNDEFINED
TERM 3	38		15-B3	UNDEFINED
TERM 4	295		15-B3	UNDEFINED
TP01	39		3-D5	
TP02	45		3-C6	
TP04	43		12-C8	
WEO/	292		3-B8	
WRITE/	290		3-D4	

NOTES (UNLESS OTHERWISE SPECIFIED)

MCN.DPD FORM NO. E-1267

INTER-DIVISIONAL DOCUMENT

Changes to this document require approval of all Using Divisions per CBC-STD 1.01.024.

AAL030

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NCR DATA PROCESSING DIVISION RANCHO BERNARDO, CALIFORNIA

UNIT: PROCESSOR

NAME: SCHEMATIC-LOGIC CARD

READER/LINE PRINTER

SHEET 2 OF 16

SCALE: NONE

96744220 A

315-053-6161

Figure 5-4. Card Reader/Line Printer (PMA 88909502 and PMA 88909503) Logic Diagram (Sheet 3 of 17)

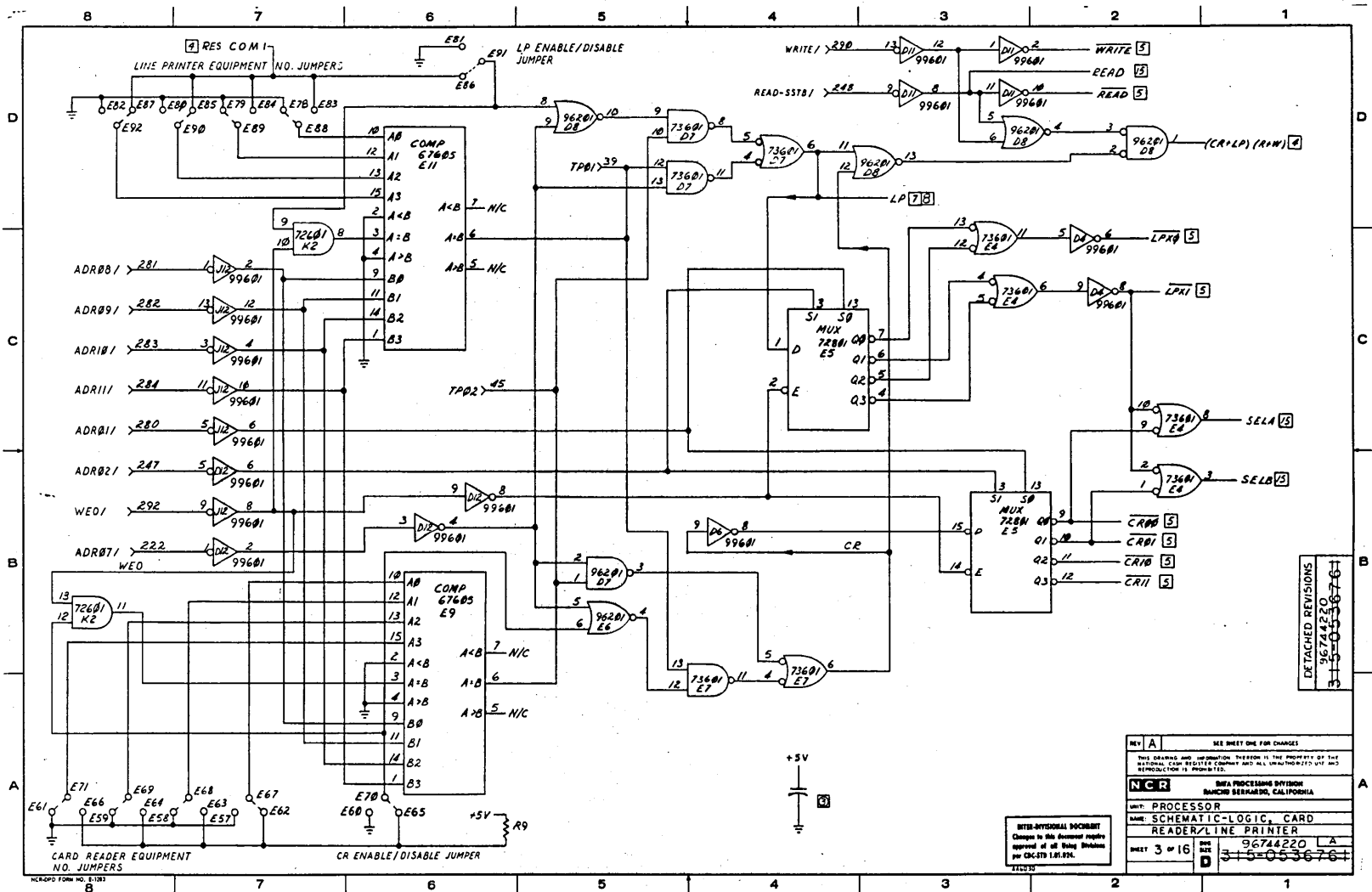


Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 4 of 17)

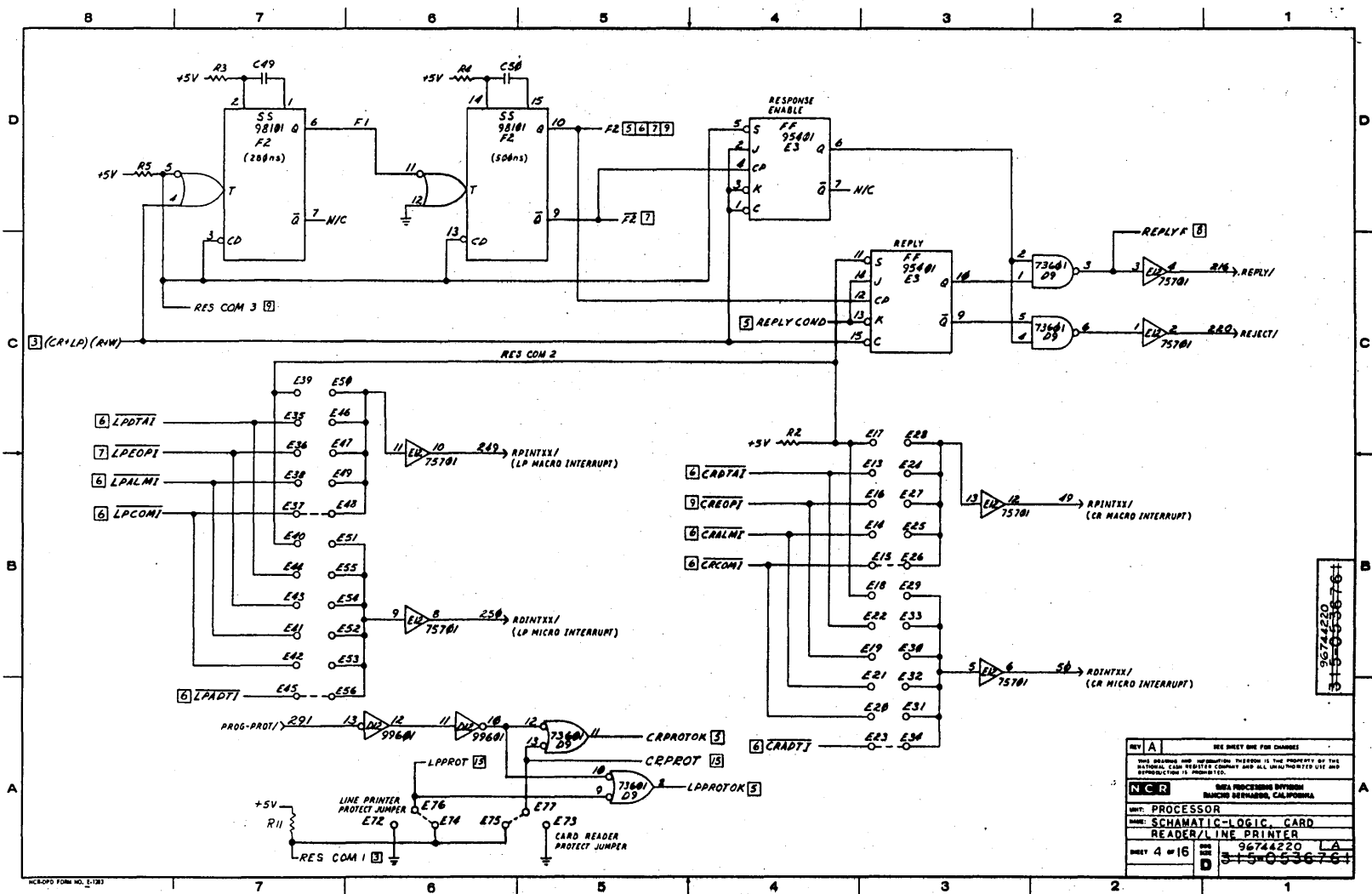


Figure 5-4. Card Reader/Line Printer (PMA 88909502 and PMA 88909503) Logic Diagram (Sheet 5 of 17)

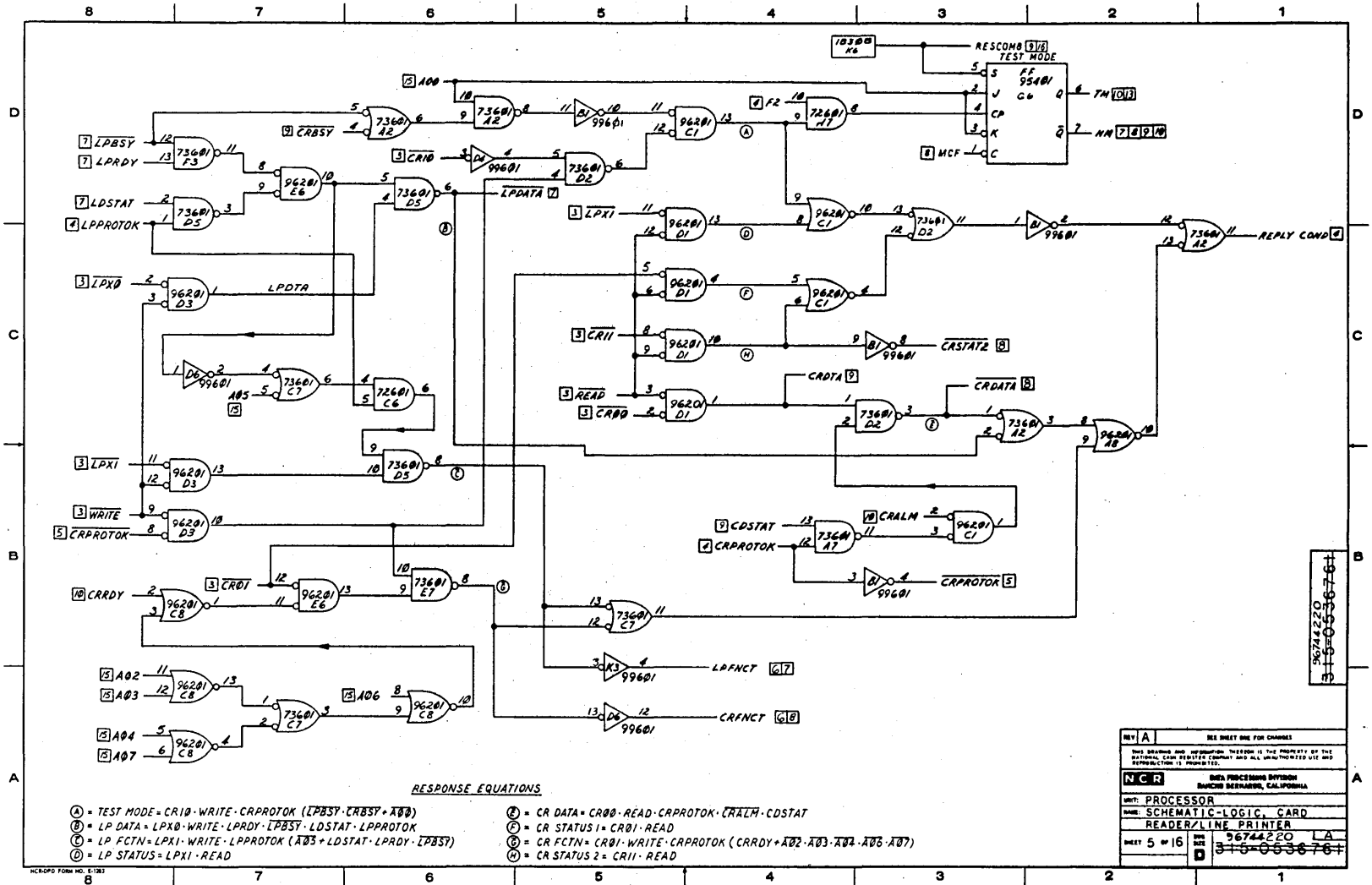
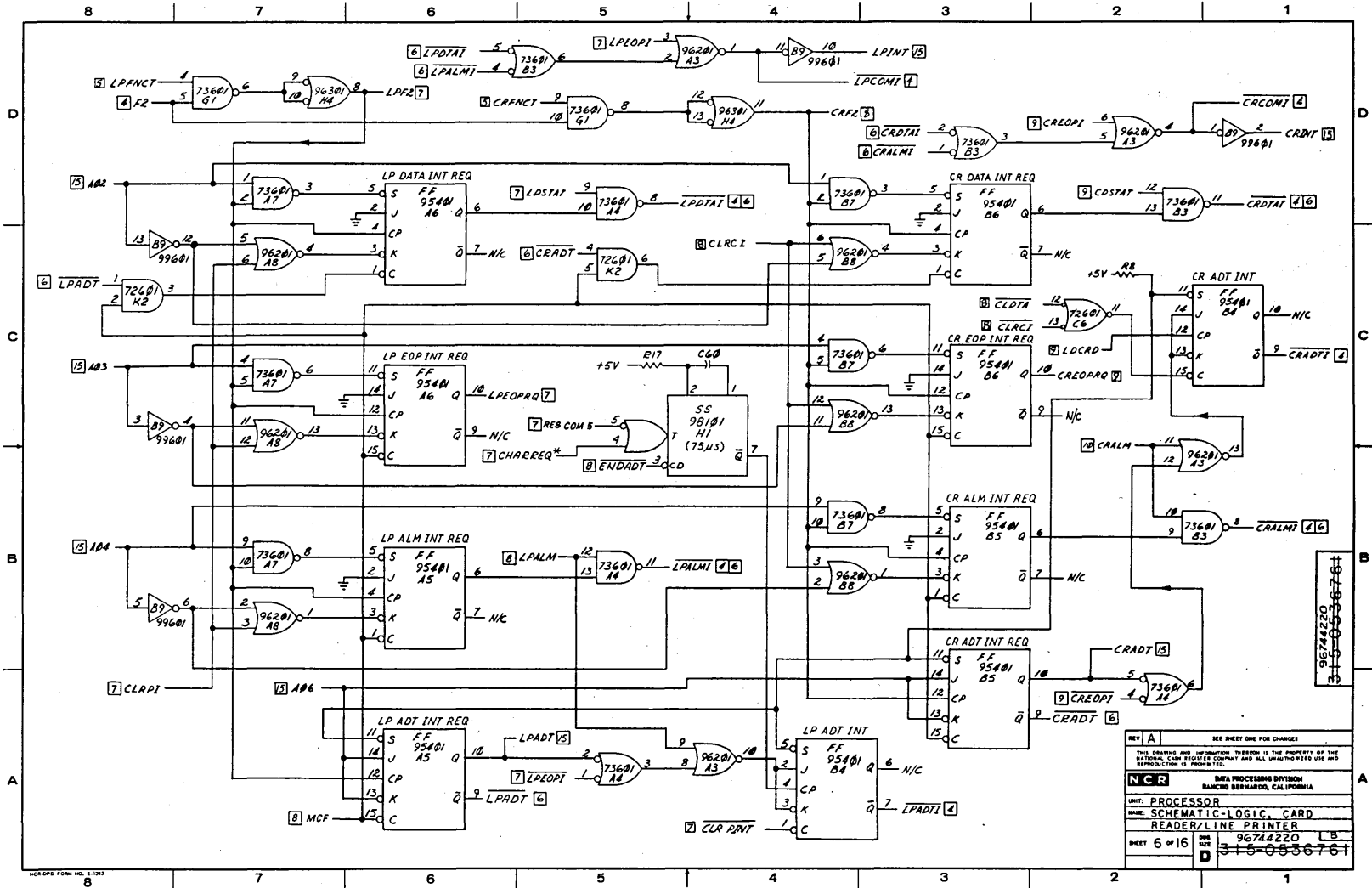


Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 6 of 17)



The schematic diagram illustrates the internal logic of the NCR 5624 Processor Logic Card. It features several key components and their interconnections:

- Input/Output Multiplexers (MUX):** Two 10A MUX units are present. The first MUX (top left) has inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D). The second MUX (bottom left) has inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (10A), 2B (10B), 2C (10C), and 2D (10D).
- Logic Functions and Flip-Flops:**
 - LP EOP INT:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP PRQ:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP I:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP O:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP I:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
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 - LP EOP O:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
- Control and Status Logic:**
 - CHAR REQ:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - RES COM:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP DATA STATUS:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP LOSTAT:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - CONTROL BIT:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP STROBE:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
- Other Logic:**
 - LP EOP INT:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP PRQ:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP I:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP O:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP I:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP O:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP I:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP O:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP I:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).
 - LP EOP O:** A 954B flip-flop with inputs 1A (N/C), 1B (10B), 1C (10C), 1D (10D), and 1E (ground). Its outputs are 2A (N/C), 2B (10B), 2C (10C), and 2D (10D).

The diagram also includes a title block with the following information:

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- DATA PROCESSING DIVISION**
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- UNIT: PROCESSOR**
- NAME: SCHEMATIC-LOGIC CARD**
- READER/LINE PRINTER**
- SHEET 7 OF 16**
- DATE: 9/6/66**
- BY: 315-05367-61**

of 17)

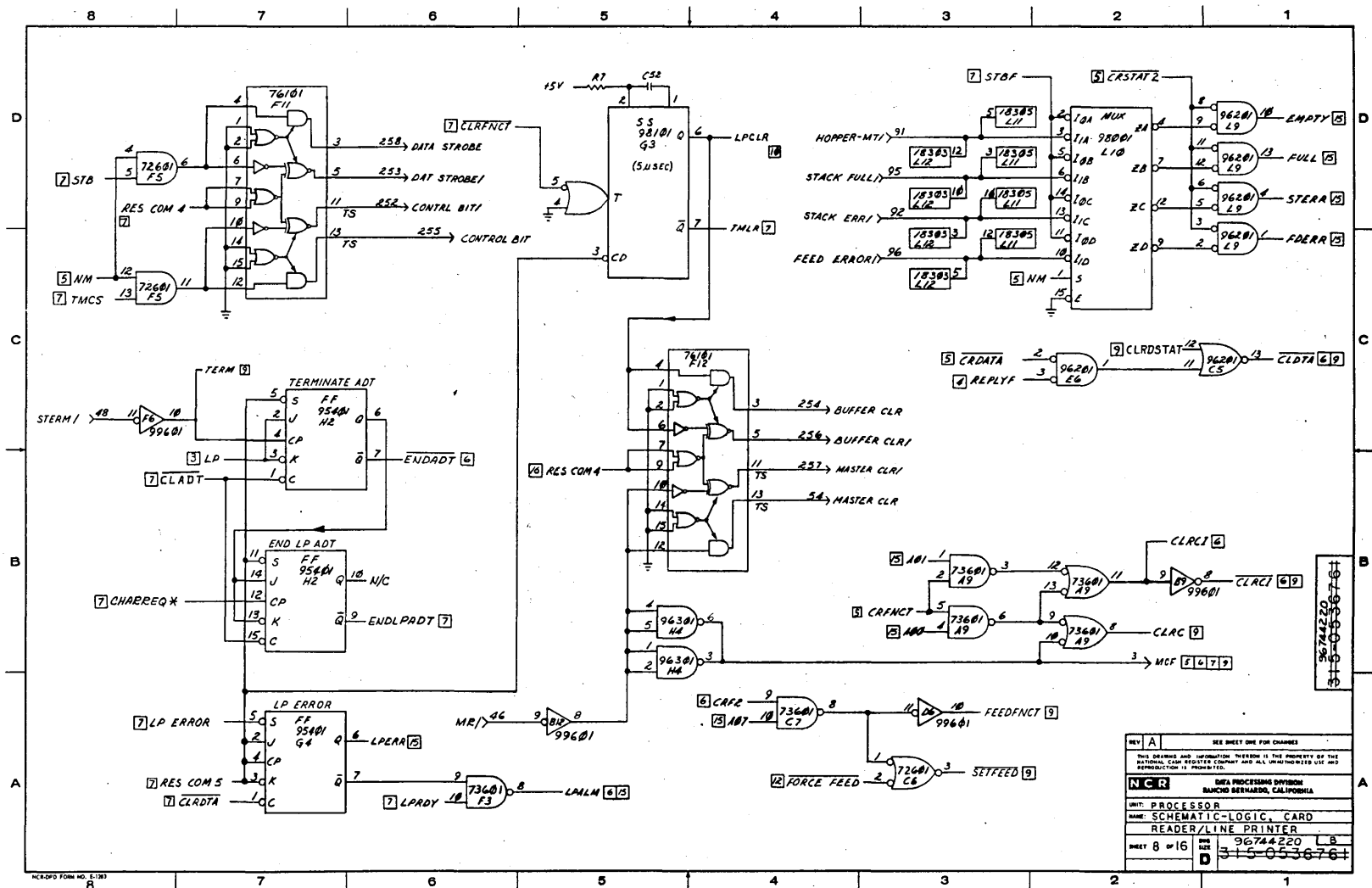


Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 9 of 17)

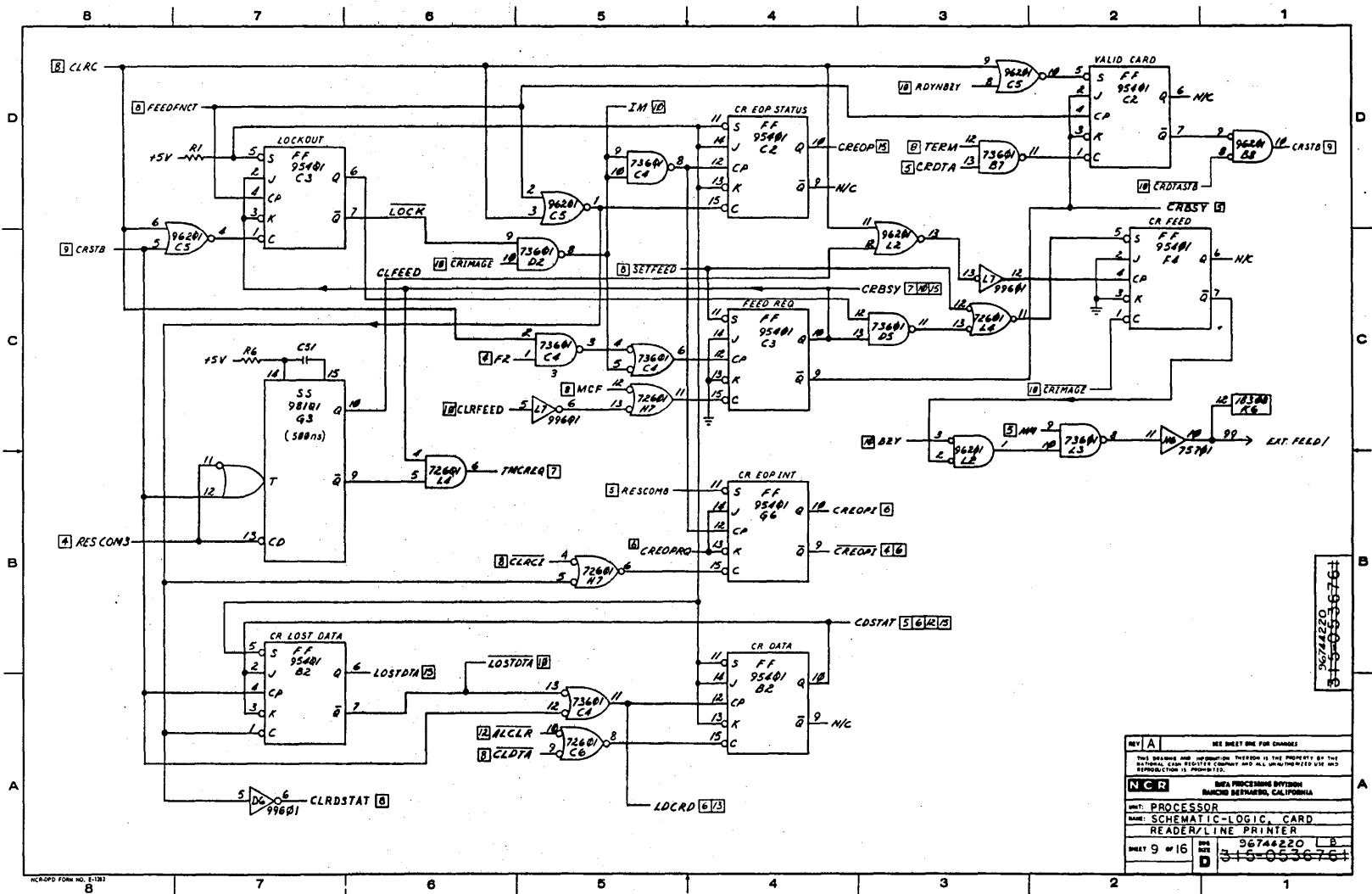
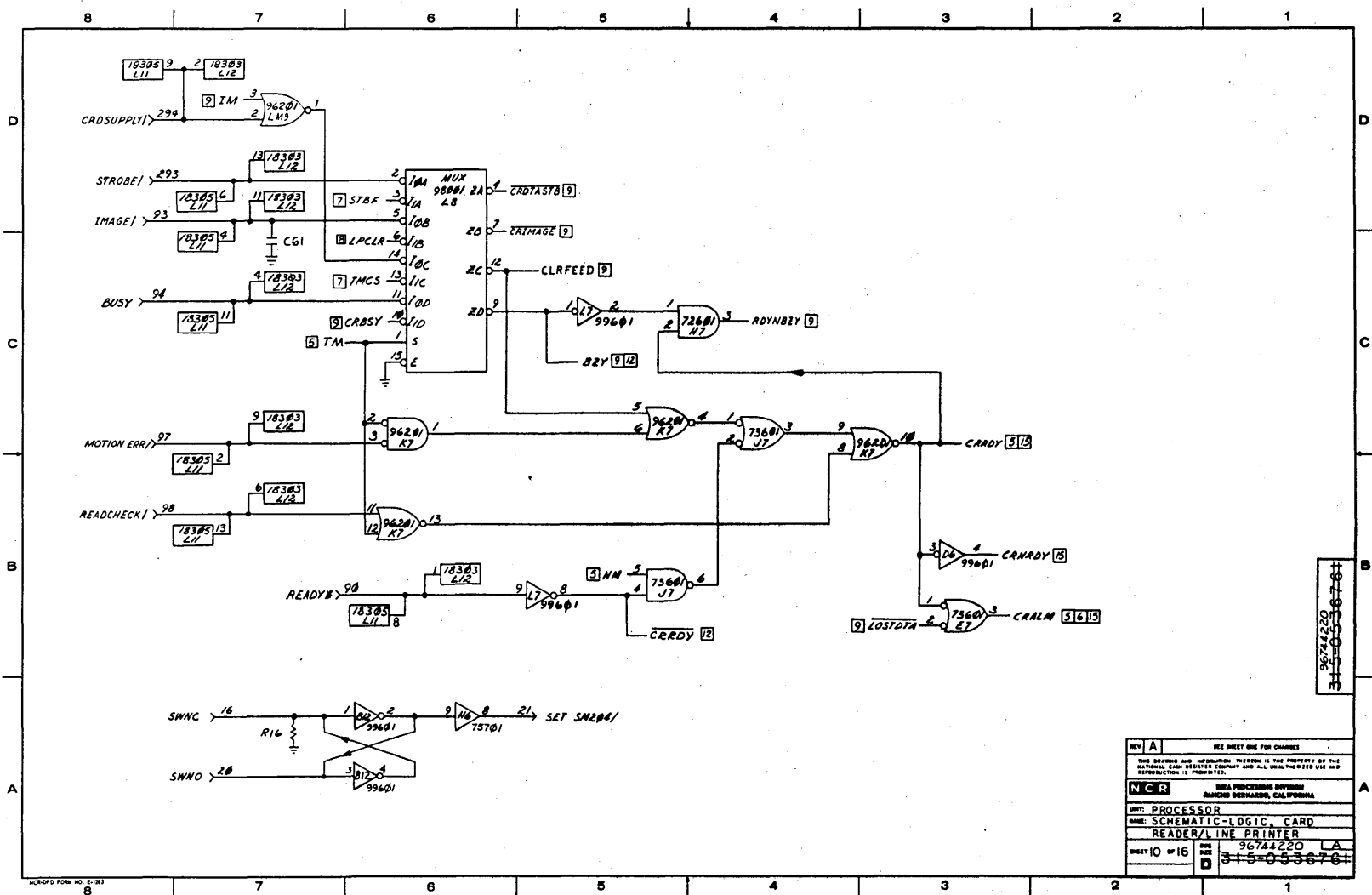


Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 10 of 17)



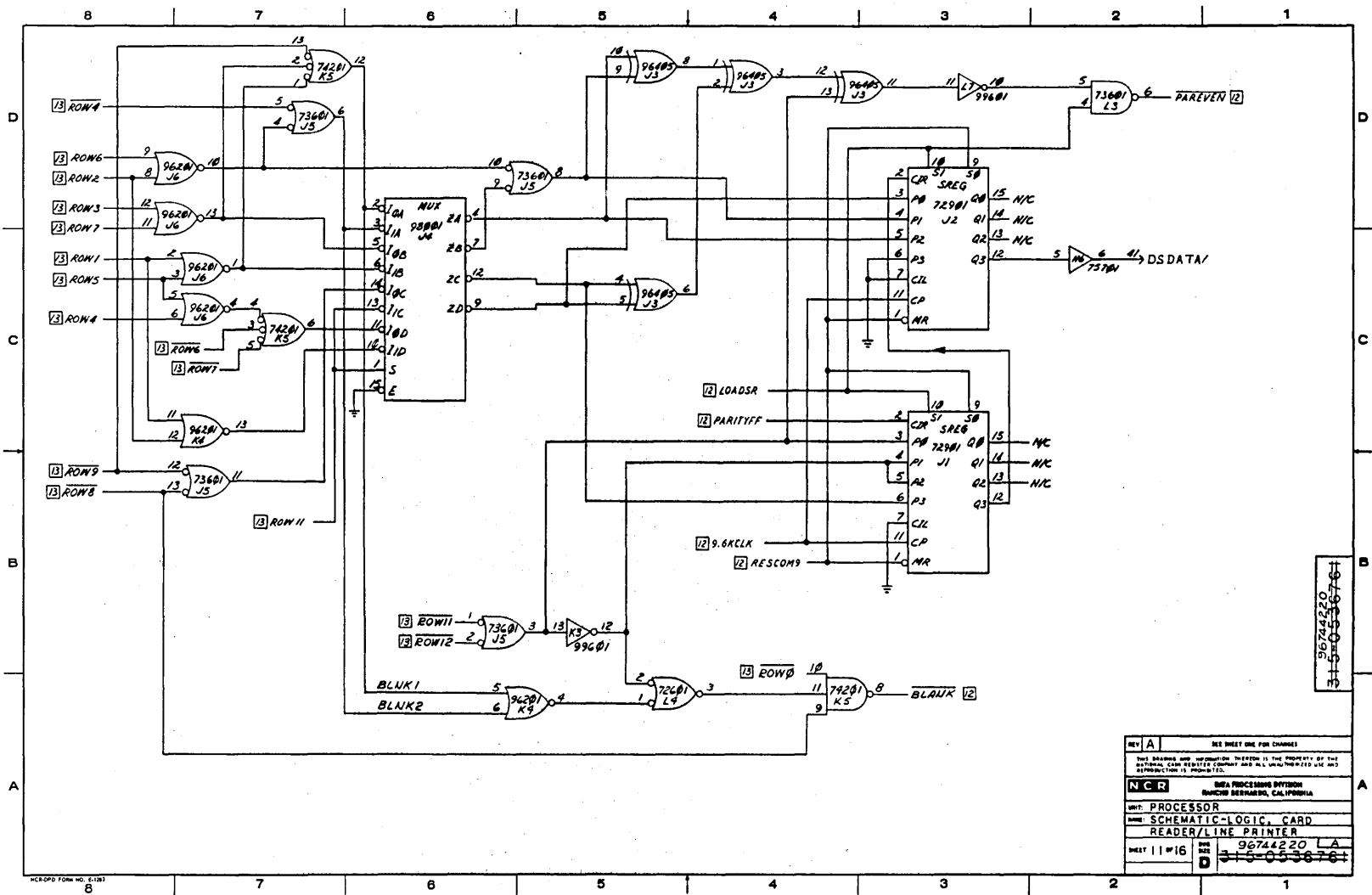


Figure 5-4. Card Reader/Line Printer (PMA 88909502 and PMA 88909503) Logic Diagram (Sheet 11 of 17)

Figure 5-4.

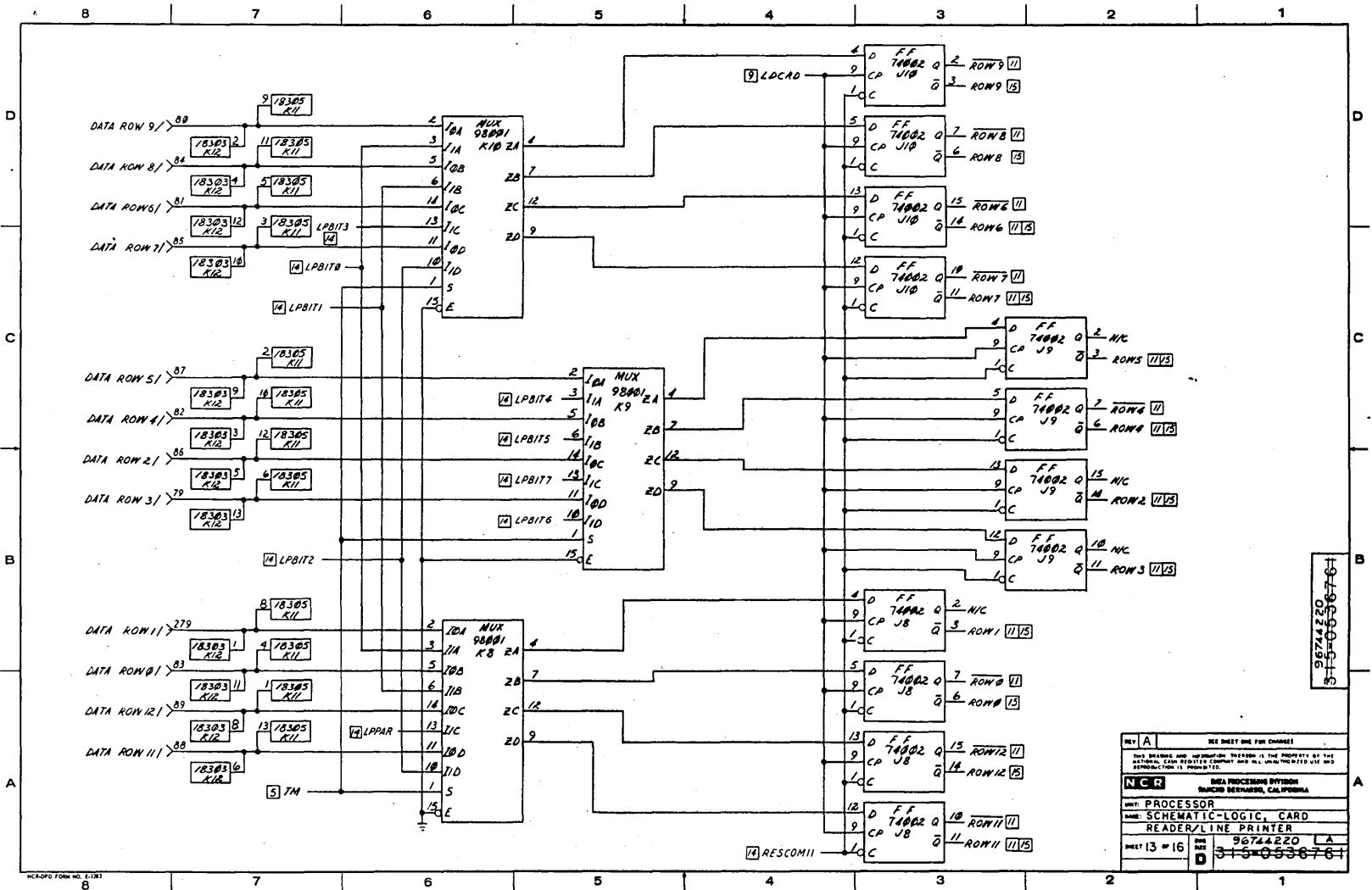


Figure 5-4. Card Reader/Line Printer (PWA 88909502 and PWA 88909503) Logic Diagram (Sheet 14 of 17)

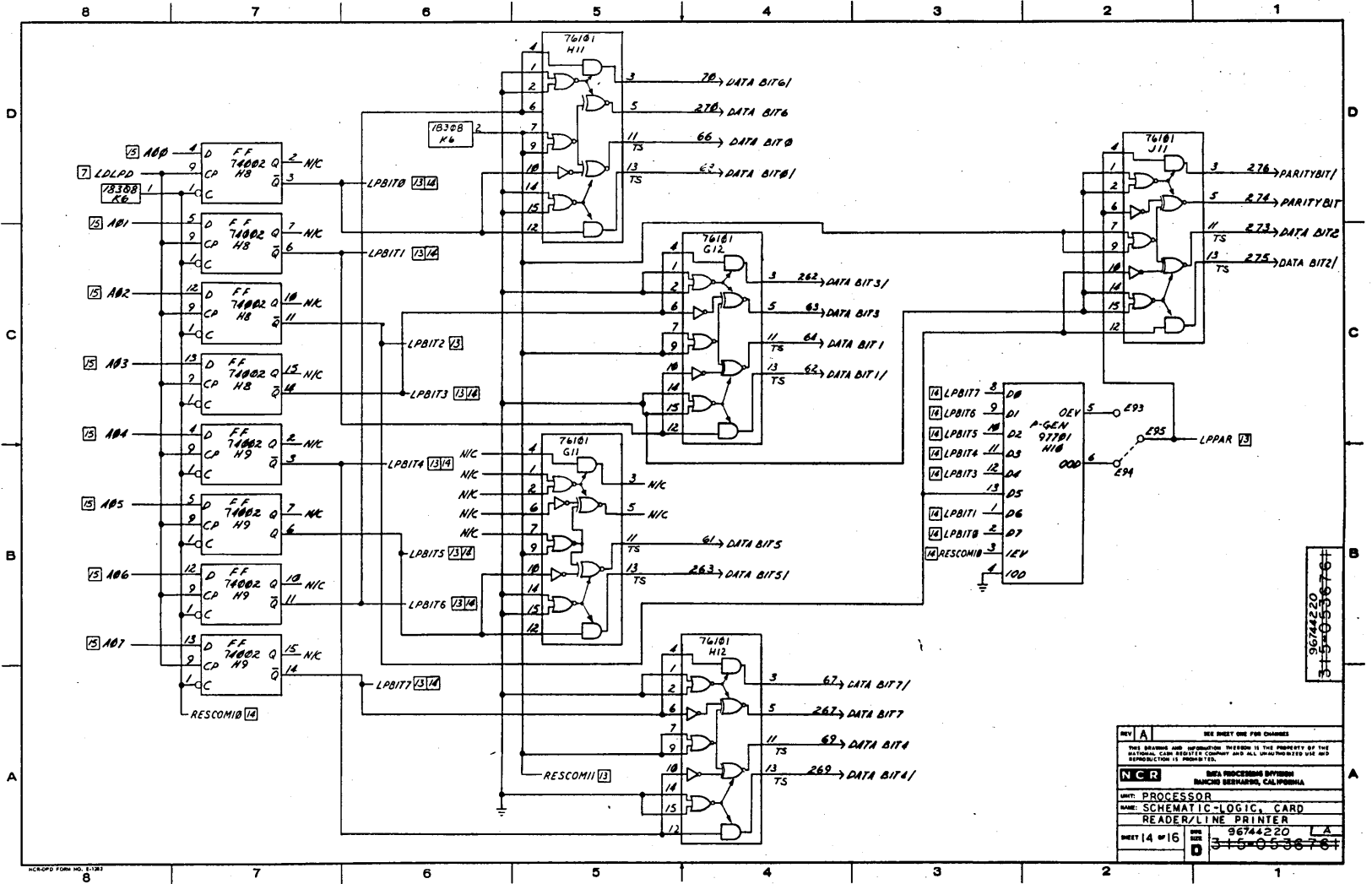


Figure 5-4. Card Reader/Line Printer (PMA 88909502 and PMA 88909503) Logic Diagram (Sheet 15 of 17)

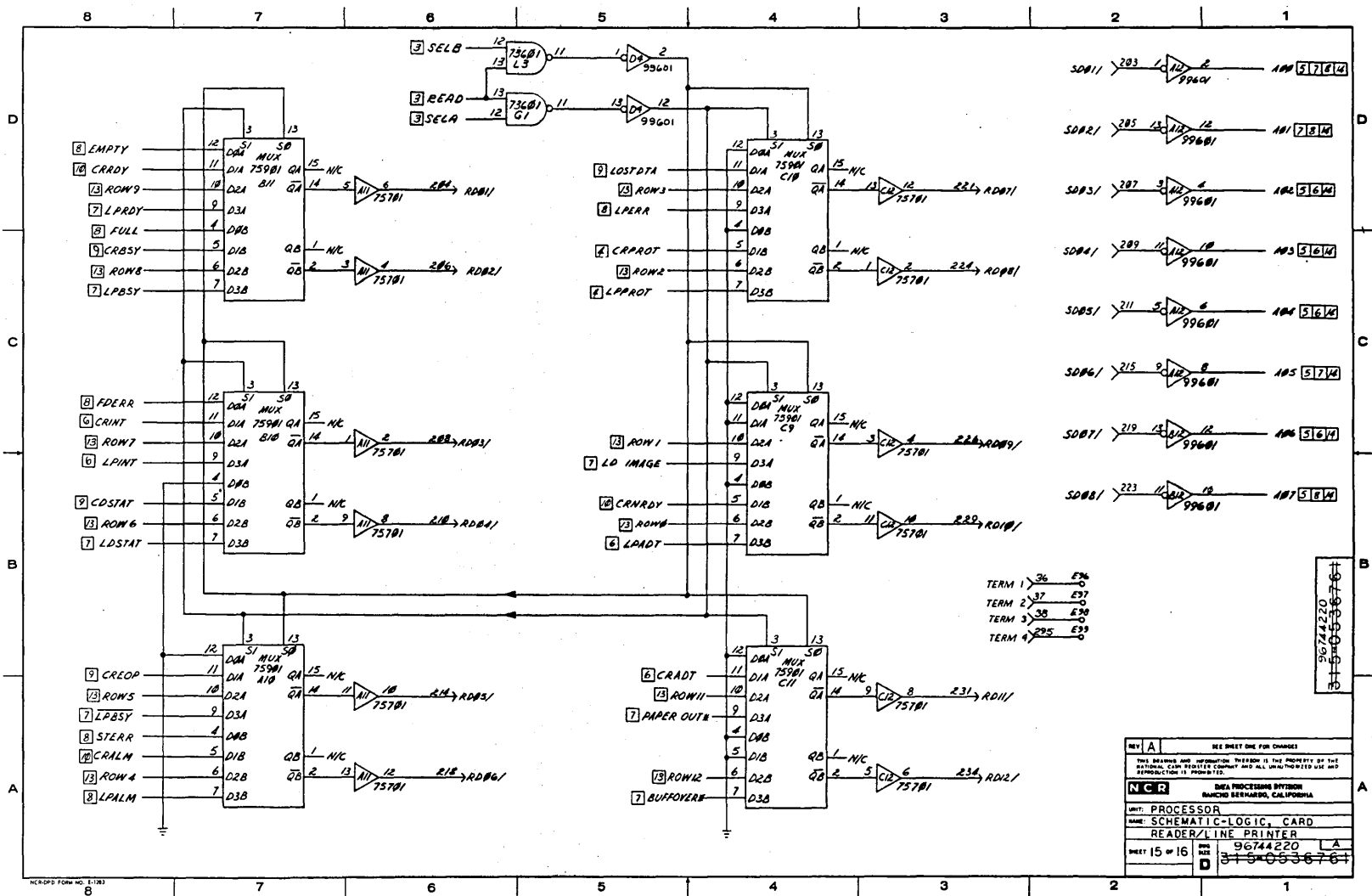
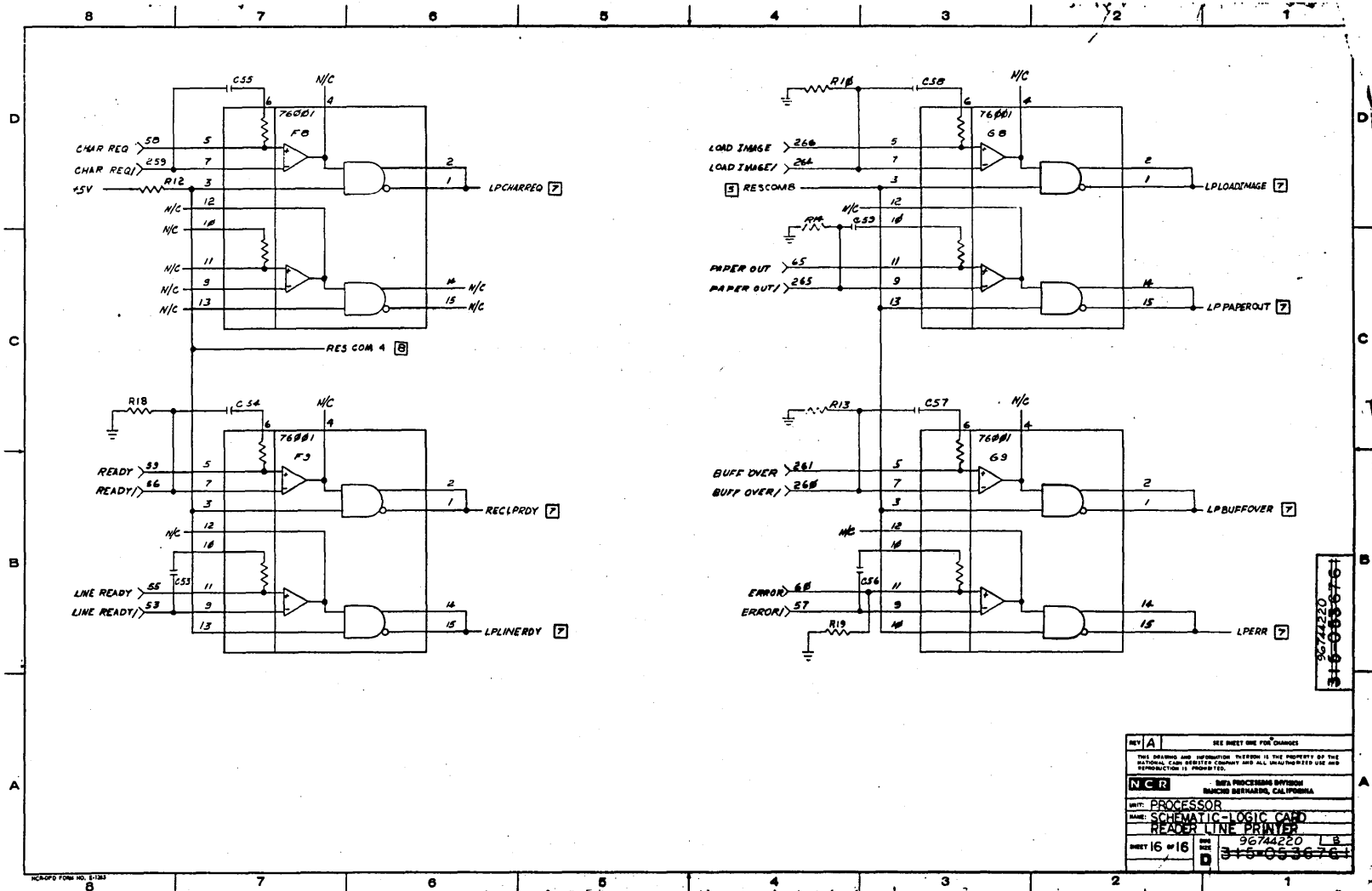


Figure 5-4. Card Reader/line Printer (PMA 88909502 and PMA 88909503) Logic Diagram (Sheet 16 of 17)



This reference/maintenance manual contains card reader/line printer logic and parts data diagrams. Diagnostic routines used to isolate controller malfunctions are documented at the system level. Therefore, the appropriate system reference manual should be consulted for diagnostic information.

COVERAGE DEPTH

This manual is written to provide information needed to isolate all problems in the equipment's logic module, backplane wiring, and interconnecting cables. Solution of problems involving this equipment's logic is limited to module replacement.

PREVENTIVE MAINTENANCE

This equipment consists of a printed circuit board that plugs into the CPU chassis. All preventive maintenance for the card reader/line printer controller is covered by the preventive maintenance procedure in the CPU manual. This consists of cleaning dirt and dust from the board while performing preventive maintenance on the CPU. No additional maintenance is required.

CARD REMOVAL

A card extractor tool (CDC part number 88911900) is used to remove the controller card. The tool is used to pry the card loose from the card cage backpanel.

TEST MODE

Test mode provides internal switching of data and control signals within the card reader/line printer controller. Figure 6-1 shows the control signal interconnections and figure 6-2 shows data bit interconnections during test mode. The signal switching occurs just in front of the transmitter and receiver interfaces to the peripherals. During test mode, control signals to and from the peripherals are disabled. Therefore, it is not necessary to remove the peripheral I/O cables during diagnostic checkout.

Diagnostic routines can test all I/O signals and most internal controller functions and status independently of the peripheral equipment. The following four sequences are sufficient to test all functions and status of both controllers. Table 6-1, 6-2, 6-3, and 6-4 show the relationship between the operations directed at the controller and the expected status and data that result.

The Operational Diagnostic System Reference Manual contains more information of the specific diagnostic routines used during test mode.

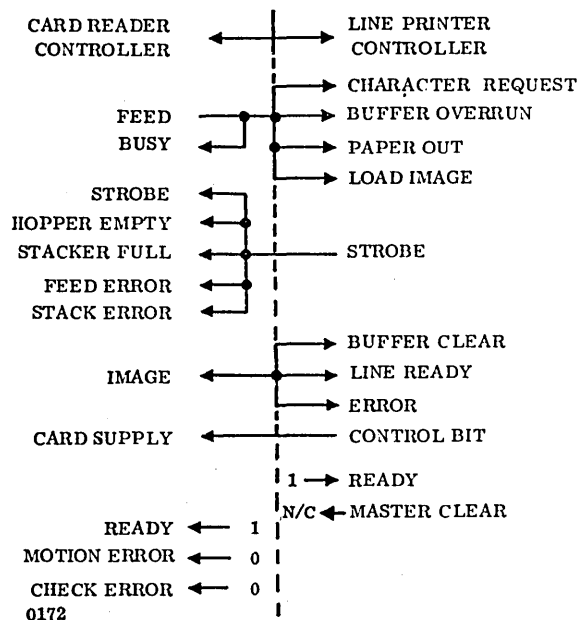


Figure 6-1. Test Mode Signal Interconnections

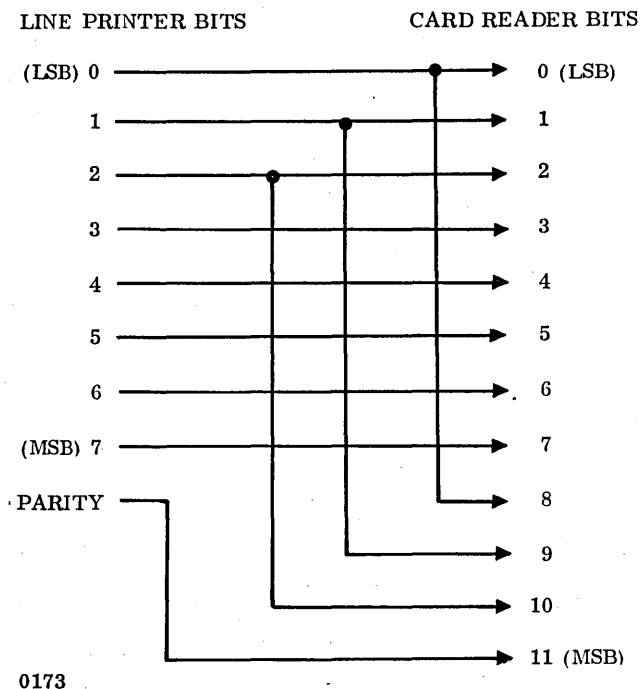


Figure 6-2. Test Mode Data Bit Interconnections

TABLE 6-1. SEQUENCE NO. 1

Output Operation	A/Q Function Code (Hexadecimal)		Card Reader Status Flags Set	Status Word (Hex)		Line Printer Status	Status Word (Hex)
	Card Reader	Line Printer		No. 1	No. 2		
1. Clear/set test mode	0	0	READY	1	0	READY EOP DATA (INDETERMINATE)	11 or 19
2. Card reader feed A/Q mode Line printer data interrupts Card reader, all interrupts	9C	4	READY BUSY	3	0	READY INTERRUPT DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D1D
3. Line printer data output A/Q mode Line printer, no interrupts Card reader data interrupts Data from line printer	4	2	READY BUSY INTERRUPT DATA	F	0	READY DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D19
4. Card reader data input A/Q mode Card reader, no interrupts Line printer, no interrupts	2	2	READY BUSY + DATA CHECK	B	0	READY DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLOW	D19
5. Auto-data transfer ADT mode Card reader alarm interrupt	D0	40	INTERRUPT DATA ALARM LOST DATA NOT READY ADT MODE	66C	0	READY EOP ADT MODE	211

TABLE 6-2. SEQUENCE NO. 2

Output Operation	A/Q Function Code (Hexadecimal)		Card Reader Status Flags Set	Status Word (Hex)		Line Printer Status	Status Word (Hex)
	Card Reader	Line Printer		No. 1	No. 2		
1. Clear/set test mode	0	0	READY	1	0	READY EOP DATA (INDETERMINATE)	11 or 19
2. CARD reader feed A/Q mode Line printer data interrupts Card reader, no interrupts	80	4	READY BUSY	3	0	READY INTERRUPT DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D1D
3. Line printer data output A/Q mode Line printer data interrupts Card reader, no interrupts	2	4	READY BUSY DATA	B	0	READY INTERRUPT DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D1D
4. Line printer data output A/Q mode Line printer, no interrupts Card reader alarm interrupts	10	2	READY BUSY INTERRUPT DATA	6F	0	READY DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D19

TABLE 6-3. SEQUENCE NO. 3

Output Operation	A/Q Function Code (Hexadecimal)		Card Reader Status Flags Set	Status Word (Hex)		Line Printer Status	Status Word (Hex)
	Card Reader	Line Printer		No. 1	No. 2		
1. Clear/set test mode	0	0	READY	1	0	READY EOP DATA (INDETERMINATE)	11
2. CARD reader feed A/Q mode Line printer data interrupts Card reader, no interrupts	80	4	READY BUSY	3	0	READY INTERRUPT DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D1D
3. Card reader feed A/Q mode Line printer data interrupts Card reader, no interrupts	80	4	READY BUSY	3	0	READY DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D19
4. Line printer data output A/Q mode Line printer, no interrupts Card reader alarm interrupts	2	2	READY BUSY HOPPER EMPTY STACKER FULL FEED ERROR STACKER ERROR	3	27	READY EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D11
5. Line printer data output A/Q mode Line printer and card reader, no interrupts	2	2	NOT CHECKED			REJECT	

TABLE 6-4. SEQUENCE NO. 4

Output Operation	A/Q Function Code (Hexadecimal)		Card Reader Status Flags Set	Status Word (Hex)		Line Printer Status	Status Word (Hex)
	Card Reader	Line Printer		No. 1	No. 2		
1. Clear/set test mode	0	0	READY	1	0	READY EOP DATA (INDETERMINATE)	11 or 19
2. Card reader feed A/Q Line printer data interrupts Card reader, no interrupts	80	4	READY BUSY	3	0	READY INTERRUPT DATA EOP LOAD IMAGE PAPER OUT BUFFER OVRFLW	D1D
3. Card reader data input A/Q mode No interrupts	2	2	REJECT			NOT CHECKED	
4. Line printer print A/Q mode Card reader alarm interrupts Line printer, no interrupt	10	22	INTERRUPT ALARM NOT READY	224	0	READY DATA EOP	19
5. Card reader illegal Line printer, no interrupts	4 8 10 40 80	0 No output	REJECT			NOT CHECKED	
6. Line printer clear Card reader, no interrupts Line printer clear, alarm interrupt	2	11	READY EOP	11	0	READY INTERRUPT EOP ALARM ERROR	75
7. Line printer print Card reader, no interrupts	2	20	NOT CHECKED			REJECT	

This section contains the card reader/line printer controller parts location and description. This

section also contains the card reader and line printer cable assembly and connector terminations.

CONDUCTOR CUT LIST

CUT NO.	CUT BETWEEN	COMP SLD SIDE
1	M2-1 POINT 1	X X
2	POINT 2 POINT 3	X X
3	C4-9 C4-13	X X
4	C5-12 C5-9	X X
5	C5-12 C5-3	X X

INTERCEPT JUMPERS (W/S)

NO.	FROM	TO	DESCRIPTION
1	E15	E26	CARD READER COMMON INTER
2	E23	E24	CARD READER ADT
3	E37	E38	LINE PRINTER COMMON INTER
4	E45	E56	LINE PRINTER ADT
5	E59	E69	CARD READER COMMON INTER
6	E65	E67	CARD READER UNIMULTI
7	E65	E68	CARD READER UNIMULTI
8	E66	E71	CARD READER UNIMULTI
9	E68	E70	ENABLE CARD READER
10	E72	E76	LINE PRINTER UNIMULTI
11	E73	E77	CARD READER UNIMULTI
12	E78	F88	CARD READER UNIMULTI
13	E82	F92	LINE PRINTER EQUIP
14	E85	E90	CARD READER UNIMULTI
15	E87	F79	CARD READER UNIMULTI
16	E86	E91	ENABLE LINE PRINTER
17	E94	E92	CARD READER UNIMULTI

NOTES:

- SEND PINS C4-9, C5-2 UP AND BOLDER JUMPER, PER ITEM 10.
- IDENTIFY WITH CDC PART NO. 'B8909503' PER ITEM 48 APPROXIMATELY AS SHOWN.
- CUT CONDUCTOR APPROXIMATELY AS SHOWN PER ITEM 10.
- ROUTE JUMPERS (WIRE)/COMPONENTS APPROXIMATELY AS SHOWN PER ITEM 10.
- IDENTIFY PER ITEM 48 APPROXIMATELY AS SHOWN.
- INSTALL FROM THIS SIDE.
- INDICATES POSITIVE POLARITY OF CAPACITOR.
- INDICATES PIN NUMBER I.

REF: R18, R19

PWA - CARD READER / LINE PRINTER

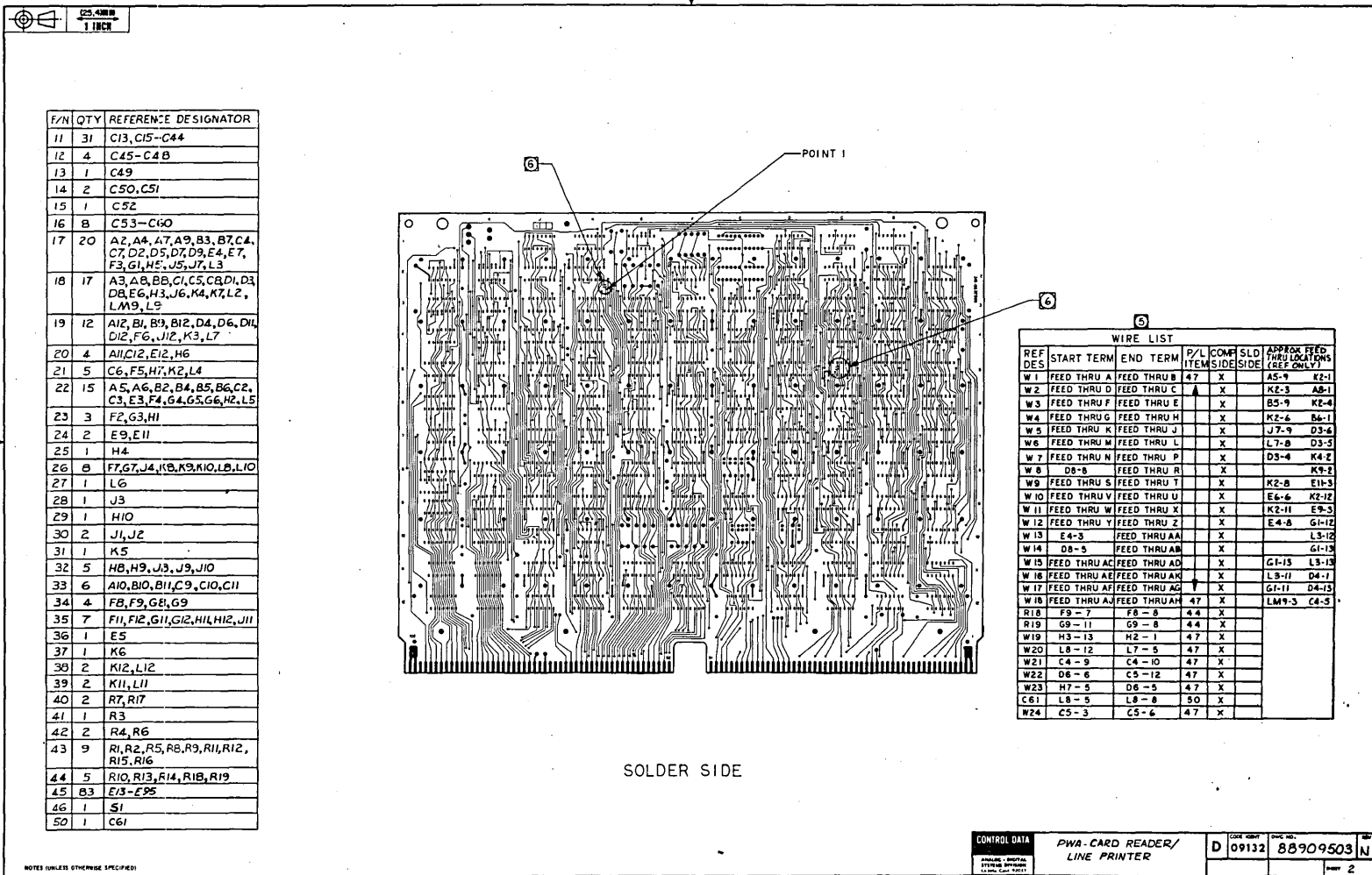
D 09132 88909503N

DATE: 1/1

SHEET 1 OF 2

Figure 7-1. Card Reader/Line Printer Printed Wiring Assembly (Sheet 2 of 5)

NOTE: PWA 88909502 does not contain capacitor C61.



DWN	D. LINVILLE	2 APR 77	CONTROL DATA	TITLE	PWA - CARD READER/ LINE PRINTER	PREFIX	DOCUMENT NO.	REV
CHKD	<i>[Signature]</i>	4-16-77				PL	88909503	N
ENG	<i>[Signature]</i>	4-20-77	SMALL COMPUTER DEVELOPMENT DIVISION	FIRST USED ON	MP17			
MFG			CODE IDENT					
APPR	<i>[Signature]</i>	4-22-77	09132					SHEET 1 OF 3

SHEET REVISION STATUS										REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	APP								
H	14435	SEE ECO	<i>[Signature]</i>	4-22-76	AW								
J	DS14955	ADDED F/N51	<i>[Signature]</i>	11-7-77	AW								
K	DS21272	REMOVED F/N4&5	<i>[Signature]</i>	6-30-78	AW								
INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC STD 1.01.034													

NOTES:

ALSO SEE

DETACHED LISTS



ASSEMBLY PARTS LIST

SPARE CODE	
S	= SPARE PARTS
N	= NON SPARE PARTS

SH 2

MF

PART NO.											
R8909503		N	CLA	D	PWA-CAPD PEADER/LINE PRINTER		OSM	MP17	09/24/75	01/27/80	1/2
ASSEMBLY NUMBER	REV	CLASS	OW	SE	ASSEMBLY DESCRIPTION			DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PAGE NUMBER
FIND NUMBER	OW	SE	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PC
43	C		24500063	900	PC	RES FXD .25W 1000 OHMS	IN	014435	041676	PPD4	N
44	C		24500075	500	PC	RES FXD .25W 3300 OHMS	IN	014435	041676	PPD4	N
41	C		24500080	100	PC	RES FXD .25W 5100 OHMS	IN	014435	041676	PPD4	N
42	C		24500083	200	PC	RES FXD .25W 6800 OHMS	IN	014435	041676	PPD4	N
40	C		24500094	200	PC	RES FXD .25W 20000 OHMS	IN	014435	041676	PPD4	N
49	C		24563702	600	IN	INSL-SLEEVING HIGH TEMP 20 GA	IN	014435	041676	PPD3	N
51	C		25195033	2000	IN	WIRE TEF INSUL 24AWG WHITE	IN	014555	101777	PPD3	N
48	A		39156108	REF	PC	SPEC-MARKING/LETTERING,OPT	IN	014435	041676	RF4	N
44	C		52629949	12000	IN	WIRE ELEC 30 GA WHITE	IN	039382	041676	PPD1	N
37	A		75009901	100	PC	RESISTOR MODULE 1K OHM 2 0/0	IN	014435	041676	PPD4	N
38	A		75009913	200	PC	RESISTOR PAC, 220 OHMS	IN	014435	041676	PPD4	N
13	A		84996715	100	PC	CAP,CER 100V 150 PF	IN	014435	041676	PPD4	N
14	A		84996717	200	PC	CAP,CER 100V 220 PF	IN	014435	041676	PPD4	N
15	A		84996727	100	PC	CAP,CER 100V 420 PF	IN	014435	041676	PPD4	N
50	A		84996730	100	PC	CAP,CER 100V 1200 PF	IN	014435	041676	PPD4	N
16	A		84996743	800	PC	CAP,CER 100V .01 MF	IN	014435	041676	PPD4	N
6	A		88812400	400	PC	RIVET-SEMI-TURULAR,BRS .312 LG	IN	014435	041676	PPD4	N
4	B		88875200	100	PC	TAR-IDENTIFICATION,CARD	IN	014435	041676	PPD4	N
4	B		88875200	100	PC	TAR-IDENTIFICATION,CARD	OUT	021222	041676	PPD4	N
7	D		88875500	600	PC	RUS RAR (13 IN)	IN	014435	041676	PPD4	N
12	A		88880500	400	PC	CAP ELECT-ALUM 16VDC 100UF	IN	014435	041676	PPD4	N
27	A		88880800	100	PC	IC 7497 TTL 4-BIT BINARY MUX	IN	014435	041676	PPD4	N
24	A		88880900	200	PC	IC 7485 TTL 4-BIT MAGN COMPAR	IN	014435	041676	PPD4	N
21	A		88881200	500	PC	IC 7449R TTL QUAD 2-INPUT AND	IN	014435	041676	PPD4	N
36	A		88881400	100	PC	IC 74155 TTL 2/4 DECODER/MUX	IN	014435	041676	PPD4	N
30	A		88881600	200	PC	IC 74194 TTL 4-BIT BIDI S REG	IN	014435	041676	PPD4	N
17	A		88882100	2000	PC	IC 74400 TTL QUAD 2-I POS NAND	IN	014435	041676	PPD4	N
32	A		88882900	500	PC	IC 74175 TTL QUAD D F/F W/CLR	IN	014435	041676	PPD4	N
31	A		88883100	100	PC	IC 74310 TTL TPL 3-1 POS NAND	IN	014435	041676	PPD4	N
20	A		88883200	400	PC	IC 7407 TTL HEX RUFFER (OC)	IN	014435	041676	PPD4	N
33	A		88883400	600	PC	IC 9309 TTL DUAL 4-INPUT MUX	IN	014435	041676	PPD4	N
34	A		88883500	400	PC	IC 9615 TTL DUAL DIFF LINE REC	IN	014435	041676	PPD4	N
35	A		88883600	700	PC	IC 8831 TRI-STATE LINE DRIVER	IN	014435	041676	PPD4	N
22	A		88884400	1500	PC	IC 9024 TTL DUAL FLIP/FLOP	IN	014435	041676	PPD4	N
18	A		88885500	1700	PC	IC 7402 TTL QUAD NOR GATE	IN	014435	041676	PPD4	N
25	A		88885600	100	PC	IC 7437 TTL QUAD 2INP NAND RFR	IN	014435	041676	PPD4	N

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INTERDIVISIONAL DOCUMENT

Figure 7-1. Card Reader/Line Printer Printed Wiring Assembly (Sheet 4 of 5)

ASSEMBLY PARTS LIST

SPARE CODE
S SPARE PARTS
N NON SPARE PARTS

SH 3

89009503	4	CLA	D	DWA-CARD HEADER/LINE PRINTER	05M	WP17	09/24/75	01/27/76	21-2
ASSEMBLY NUMBER	REV	CLASS	DN	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER

MF

FIND NUMBER	QTY	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH	ON
28	A	88885700	100	PC	IC 7404 TTL QUAD 2-IN EXCL OR	IN	014435	04/16/76	PPP4	N	
29	A	88886300	100	PC	IC 74160 TTL 4-BIT PARITY GEN	IN	014435	04/16/76	PPP4	N	
26	A	88886400	800	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN	014435	04/16/76	PPP4	N	
23	A	88886500	300	PC	IC 9402 TTL DUAL MONOSTAB WVP	IN	014435	04/16/76	PPP4	N	
19	A	88886600	1200	PC	IC 7404 TTL HEX INVERTER	IN	014435	04/16/76	PPP4	N	
8	A	88887600	100	PC	LABEL IDENTIFICATION-K26	IN	014435	04/16/76	PPP4	N	
39	A	88888500	200	PC	LABEL IDENTIFICATION-K26	OUT	021722	05/07/78	PPP4	N	
45	A	88889200	8300	PC	RES NETWORK-14 PIN DIP, 510 OHM	IN	014435	04/16/76	PPP4	N	
46	A	88889300	100	PC	SOCKET-SPR, MINI .017-.019 PIN	IN	014435	04/16/76	PPP4	N	
10	A	88889500	REF	PC	SWITCH-SUP, MINI, SPDT, TOGGLE	IN	014435	04/16/76	PPP4	N	
2	D	88889600	100	PC	SPEC-PC BOARD ASSY	IN	014435	04/16/76	RFE4	N	
3	C	88889500	100	PC	STIFFENER-PC BOARD (CASTING)	IN	014435	04/16/76	PPP4	N	
11	A	88889700	3100	PC	INSULATOR-CARD STIFFENER	IN	014435	04/16/76	PPP4	N	
1	A	96744219	100	PC	CAP-FIXED SOLID TANT, +VDC, 12UF	IN	014435	04/16/76	PPP4	N	
8	D	96744220	REF	PC	PWR-CARD HEADER/LINE PRINTER	IN	014435	04/16/76	PPP4	N	
				PC	LOGIC-CARD HEADER/LINE PRINTER	IN	014435	04/16/76	RFE4	N	
NUMBER OF LINE ITEMS = 52											
HIGHEST FIND NUMBER = 51											

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PROJECT ENGINEER

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INTERDIVISIONAL DOCUMENT

Figure 7-1. Card Reader/Line Printer Printed Wiring Assembly (Sheet 5 of 5)

TABULATION			REVISION RECORD						
PART NO.	LG/IN	TOL ±	REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
88894500	180	7							
88894501	120	5							
88894502	84	3							

FOR REV SEE SH 13

4. STRIP BACK ENOUGH INSULATION TO BRAID APPROX 3 IN. OF SHIELD AND CONNECT AS SHOWN IN DETAIL D.

5. AT "B" END OF CABLE, TIE UNUSED PAIRS TOGETHER AND RUN ONE WIRE TO GND PIN 11.

6. BAG CABLE CLAMP, B-32 SCREW, FLAT WASHER, U-CAMP, AND LOCKWASHERS (F/N 19, 20, 21, 23, 24, 25) AND ATTACH TO CABLE.

3. WHT WIRE OF EACH TWISTED PAIR & EACH UNUSED PAIR TIES TO GROUND BUS (F/N 12) AT "A" END.

2. USING F/N 12 CONNECT PINS 78, 278, 102 & 302, SOLDER CRIMP CONTACTS TO F/N 12.

1. IDENTIFY CABLE PER ENG STD 1.30.008

NOTES:

INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.	DWN	1-17-74	CONTROL DATA TITLE CABLE ASSY - I/O CARD READER (MP '7) SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037	CODE IDENT		DWG NO	
	CHKD	1-17-74		09132		A 88894500/02 N	
	ENG	1-17-74					
	MFG	1-17-74					
	APP	1-17-74					

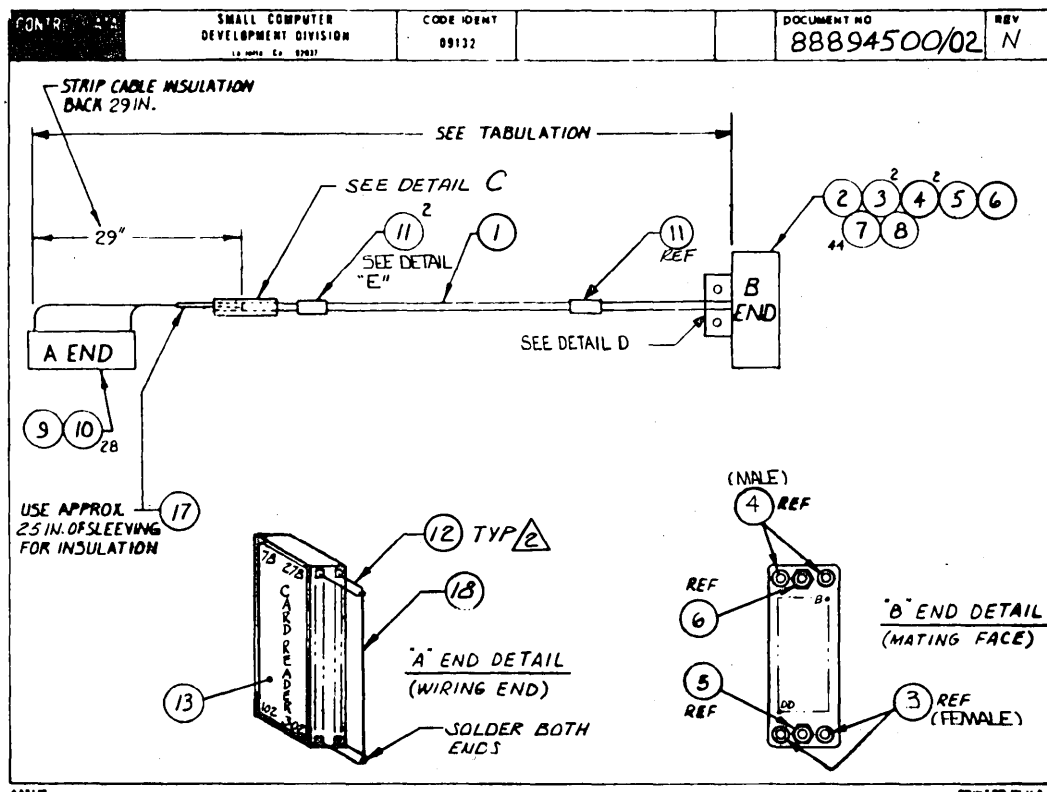
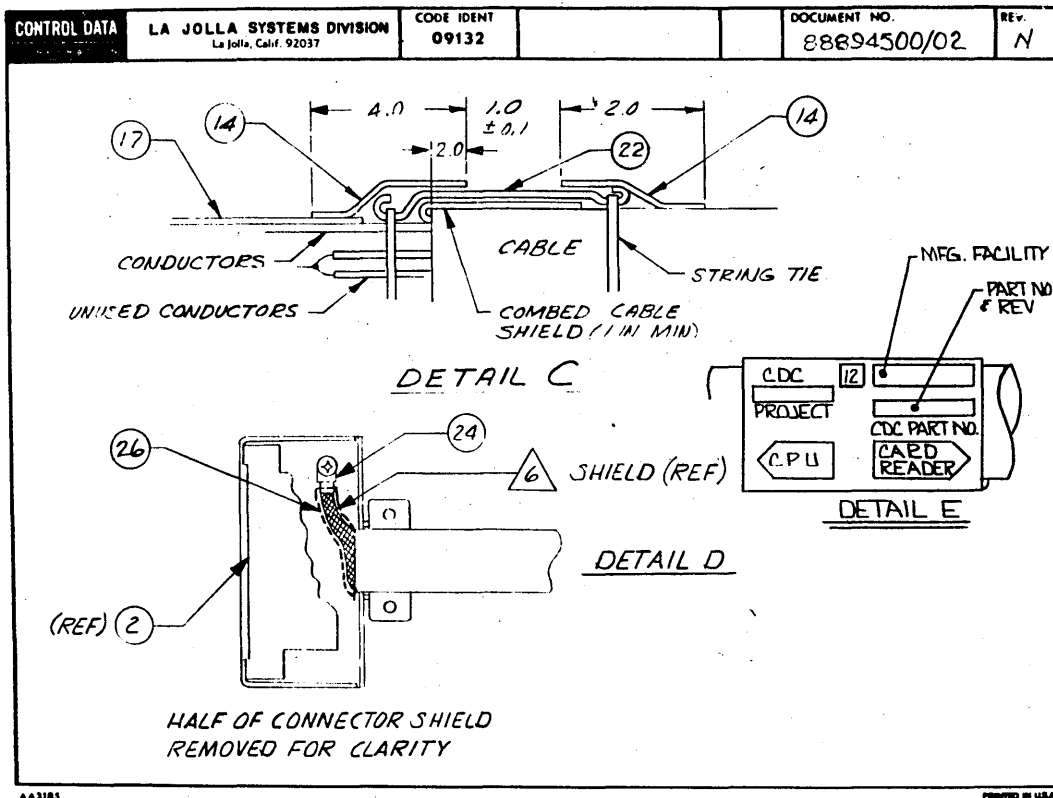


Figure 7-2. I/O Card Reader Cable Assembly (88894500) (Sheet 1 of 4)



CONTROL DATA CORPORATION		SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, Calif. 92037			CODE IDENT 09132		WL		DOCUMENT NO 88894500/02		REV K	
CONDUCTOR IDENT	FIND NO	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN		ACCESS FIND NO		DESTINATION		ACCESS FIND NO	REMARKS
1	1	24	0		A - FND	99	10	B - END	C	7	TWISTED PAIR 	
2	↑	↑	9			GND B		↑	H	↑	(TYP)	
3	↑	↑	2			90	10	↑	n	↑		
4	↑	↑	9			GND B		↑	t	↑		
5	↑	↑	4			94	10	↑	A	↑		
6	↑	↑	9			GND B		↑	E	↑		
7	↑	↑	5			98	10	↑	D	↑		
8	↑	↑	9			GND B		↑	J	↑		
9	↑	↑	6			293	10	↑	B	↑		
10	↑	↑	9			GND B		↑	F	↑		
11	↑	↑	90			93	10	↑	M	↑		
12	↑	↑	9			GND B		↑	S	↑		
13	↑	↑	91			83	10	↑	f	↑		
14	↑	↑	9			GND B		↑	m	↑		
15	↑	↑	92			279	10	↑	K	↑		
16	↑	↑	9			GND B		↑	P	↑		
17	↑	↑	93			86	10	↑	N	↑		
18	↑	↑	9			GND B		↑	T	↑		
19	↓	↓	94			79	10	↓	L	↓		
20	1	24	9		A - FND	GND F		A - END	R	7		

Figure 7-2. I/O Card Reader Cable Assembly (88894500) (Sheet 2 of 4)

DWN	1/1/73	11-7-3	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO	REV
CHKD	Guy B. B. B.	11-7-3	1A JOLLA DIVISION	CABLE, I/O-CARD READER (MP17)	PL	88894500/02	J
ENG	1/1/73	11-7-3	1A JOLLA DIVISION	FIRST USED ON			
MFG			CODE IDENT	YA119-A			
APPR			09132				

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	APP		
01		CL B PRE-RELEASED	D.M.	11/13/73	E		
02	DDC	ADDED PART No.5 (ECR4998)	D.M.	11/19/73	E		
03	DDC	ADDED PART No. (ECR5001)	D.M.	12/7/73	E		
04	DDC	ADDED TAB 01, 02 (ECR5002)	D.M.	1/2-4	E		
05	12/1/76	ADDED TO COMMAND	D.M.	12-19-76	E		
06	13/1/76	ADDED PART No's	D.M.	12/19/76	E		
07	13204	CHANGE F/N 1	D.M.	12/19/76	E		
A	13244	CL A RELEASE	JM	4-17-74	E		
B	13526	REVISED SH 21 PL	LVP	3-7-75	E		
C	14129	SEE ECO	JM	5-13-75	E		
D	14176	ADDED NOTE 4; ADDED F/N 19-21	LVP	8-25-75	E		
E	14232	REVISED PER ECO	KEW	10-8-75	E		
F	14325	REVISED PER ECO	KEW	2-6-76	E		
G	14512	SEE ECO	KEW	8-26-76	E		
H	14719	SEE ECO	KEW	12-22-76	E		
J	DS14848	00-02, 5/N 12 WAS 24501801	MRC	7-26-77	E		

NOTES: SEE SHEET 14 FOR FURTHER REVISIONS

DETACHED LISTS

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DWN	J HUMPHREYS	4-20-78	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO	REV
CHKD			1A JOLLA DIVISION	CABLE ASSY - I/O CARD READER (MP17)		88894500/02	N
ENG			DATA SYSTEMS	FIRST USED ON			
MFG			1A JOLLA DIVISION	YA119-A			
APPR			09132				

SHEET REVISION STATUS				REVISION RECORD			
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP	
K	DS21006	SEE ECO	JSH	1-1-78			
L	DS21211	SEE ECO	TVH	1-1-78			
M	DS21530	SEE ECO	VB	7-16-79			
N	DS21808	SEE ECO	KB	2-4-80			

NOTES:

DETACHED LISTS

AA2100 REV. 8/71

PRINTED IN U.S.A.

Figure 7-2. I/O Card Reader Cable Assembly (88894500) (Sheet 4 of 4)

TABULATION			REVISION RECORD						
PART NO.	LG./IN.	TOL ±	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
96870916	88	5	A	DS19165	CL. A. RELEASED	ED	8-16-77	/	GP
96870917	124	6	B	DS21759	SEE ECO	UAB	10-3-77	/	AW
96870918	184	7	C	DL72027	ADDED NOTE II & TABLE I	KB	12-16-80	/	AW

NOTES CONT'D SH 2

3 WHT WIRE OF EACH TWISTED PAIR & EACH UNUSED PAIR TIES TO GROUND BUS (F/N 2) AT "A" END.

2 USING F/N 1 & 2 CONNECT PINS 78, 278, 102 & 302, SOLDER CRIMP CONTACTS TO F/N 1.

1 IDENTIFY PER CDC STD. 1.30.008.

NOTES:

INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.	DWN	J. L. Carr	3-2-79	CONTROL DATA DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA 92037	TITLE CABLE ASSY - I/O CARD READER (CY 18)				
	CHKD	J. L. Carr	3-2-79		CODE IDENT 09132	DWG No A 96870916/18			
	ENG	J. L. Carr	3-2-79						
	MFG	J. L. Carr	7-17-79						
	APP								
				SCALE					

AA6030

GD	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132		DOCUMENT NO 96870916/18	REV C
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NOTES CONT'D :

4. BAG U-CLAMP (F/N 23) AND ATTACH TO CABLE.

5 AT "B" END OF CABLE, SOLDER UNUSED WIRES TOGETHER, SLEEVE WITH 1 IN. F/N 6, AND RUN ONE WIRE F/N 24 TO GND PIN 2.

6 STRIP BACK 2.5 IN. OF INSULATION AND BRAID APPROX 2.5 IN. OF SHIELD, SLEEVE WITH 2.25 IN F/N 7 & CONNECT AS SHOWN IN DETAIL D.

7 FOLD END OF BRAIDED SLEEVING (F/N 21) INWARD TO FORM "FISHMOUTH", FASTEN THIS END CLOSE TO SHRINK SLEEVING WITH CABLE TIE. THEN FORM FISHMOUTH AT OTHER END, AND STRETCH AND SMOOTH THE SLEEVING DOWN ITS ENTIRE LENGTH TOWARDS THE "A" END. BEFORE TIE WRAPPING THAT END, CHECK FOR 2 IN. SPACING AND ADJUST AS NECESSARY THE AMOUNT OF SLEEVING FOLDED INTO THE FISHMOUTH.

8 INSTALL LABEL (F/N 9) AFTER WIRING IS COMPLETED.

9 FILL ALL UNUSED CAVITIES OF F/N 18 WITH CRIMPED CONTACTS (F/N 13).

10 FILL ALL UNUSED CAVITIES OF F/N 3 WITH CRIMPED CONTACTS (F/N 12).

11 UNLESS OTHERWISE SPECIFIED, ALL NOMINAL DIMENSIONS COMPLY WITH TABLE 1.

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Figure 7-3. I/O Card Reader Cable Assembly (96870916) (Sheet 1 of 4)

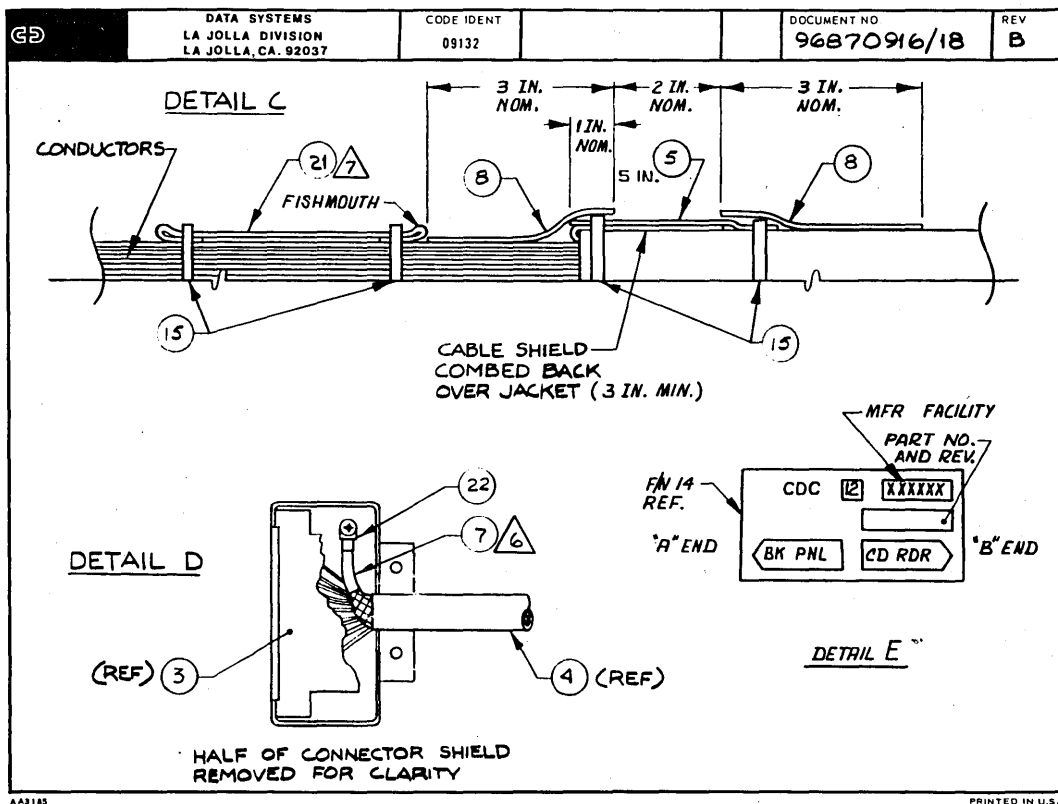
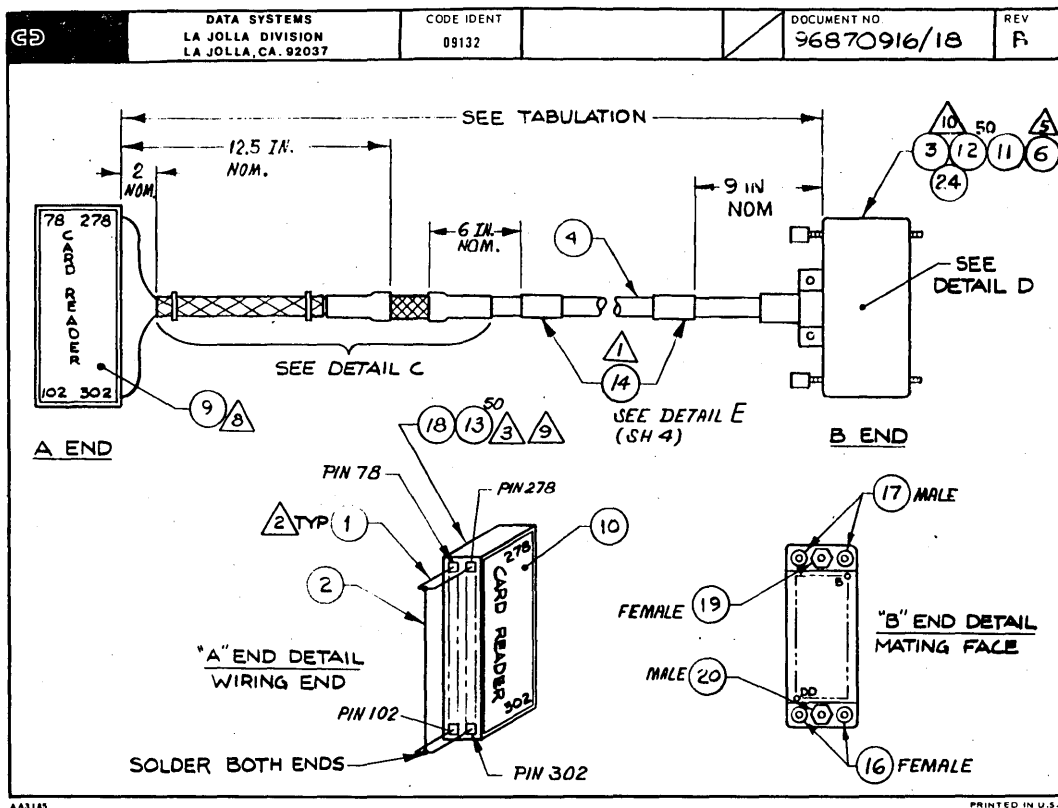


Figure 7-3. I/O Card Reader Cable Assembly (96870916) (Sheet 2 of 4)

CONTROL DATA				SMALL COMPUTER DEVELOPMENT DIVISION LA 10114 CA 92037		CODE IDENT 09132		WL		DOCUMENT NO 96870916/18		REV 2
CONDUCTOR IDENT	FIND NO	GAUGE (REF 1)	COLOR (REF 1)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS	
1	1	24	0		A- END	99	13	B- END	C	12	TWISTED PAIR  (TYP)	
2	↑	↑	9		↑	GNDB		↑	H	↑		
3			2			90	13		n			
4			9			GNDB			t			
5			4			94	13		A			
6			9			GNDB			E			
7			5			98	13		D			
8			9			GNDB			J			
9			6			293	13		B			
10			9			GNDB			F			
11			90			93	13		M			
12			9			GNDB			S			
13			91			83	13		F			
14			9			GNDB			m			
15			92			279	13		K			
16			9			GNDB			P			
17			93			86	13		N			
18			9			GNDB			T			
19	↓	↓	94		↓	79	13	↓	L	↓		
20	1	24	9		A- END	GNDB		B- END	R	12		

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CONTROL DATA				SMALL COMPUTER DEVELOPMENT DIVISION LA 10114 CA 92037		CODE IDENT 09132		WL		DOCUMENT NO 96870916/18		REV 2
CONDUCTOR IDENT	FIND NO	GAUGE (REF 1)	COLOR (REF 1)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS	
21	1	24	95		A- END	82	13	B- END	W	12		
22	↑	↑	9		↑	GNDB		↑	a	↑		
23			96			87	13		U			
24			9			GNDB			Y			
25			97			81	13		X			
26			9			GNDB			b			
27			98			85	13		V			
28			9			GNDB			Z			
29			900			84	13		e			
30			9			GNDB			k			
31			910			80	13		c			
32			9			GNDB			h			
33			920			88	13		d			
34			9			GNDB			j			
35			930			89	13		r			
36			9			GNDB			v			
37			940			91	13		u			
38			9			GNDB			w			
39	↓	↓	950		↓	95	13	↓	y	↓		
40	1	24	960		A- END	294	13	B- END	z	12		

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Figure 7-3. I/O Card Reader Cable Assembly (96870916) (Sheet 3 of 4)

TABULATION			REVISION RECORD						
PART NO.	LG/IN	TOL ±	REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
88894600	240	10							
88894601	360	14							
88894602	480	19							
88894605	600	24							

FOR REV SEE SH 11

4 TIE UNUSED PAIRS AT "B" END TOGETHER & RUN ONE WIRE TO PIN X.

3 TIE UNUSED PAIRS AT "A" END TOGETHER & RUN ONE WIRE TO PIN 76.

2 BAG CABLE CLAMP (F/N 17), U-CLAMP (F/N 21), 8-32 SCREW (F/N 18), FLAT WASHER (F/N 19) & ATTACH TO CABLE.

1. IDENTIFY CABLE PER ES38876000.

NOTES:

INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.			DWN	1-17-74	CONTROL DATA	TITLE	CABLE ASSY - I/O LINE PRINTER (MP17)		
CHKD	1-23-74		ENG	2-19-74	SMALL COMPUTER DEVELOPMENT DIVISION La Jolla, CA 92037	CODE IDENT	09132	DWG NO	88894600-03
MFG			APP	2-19-74		SCALE			

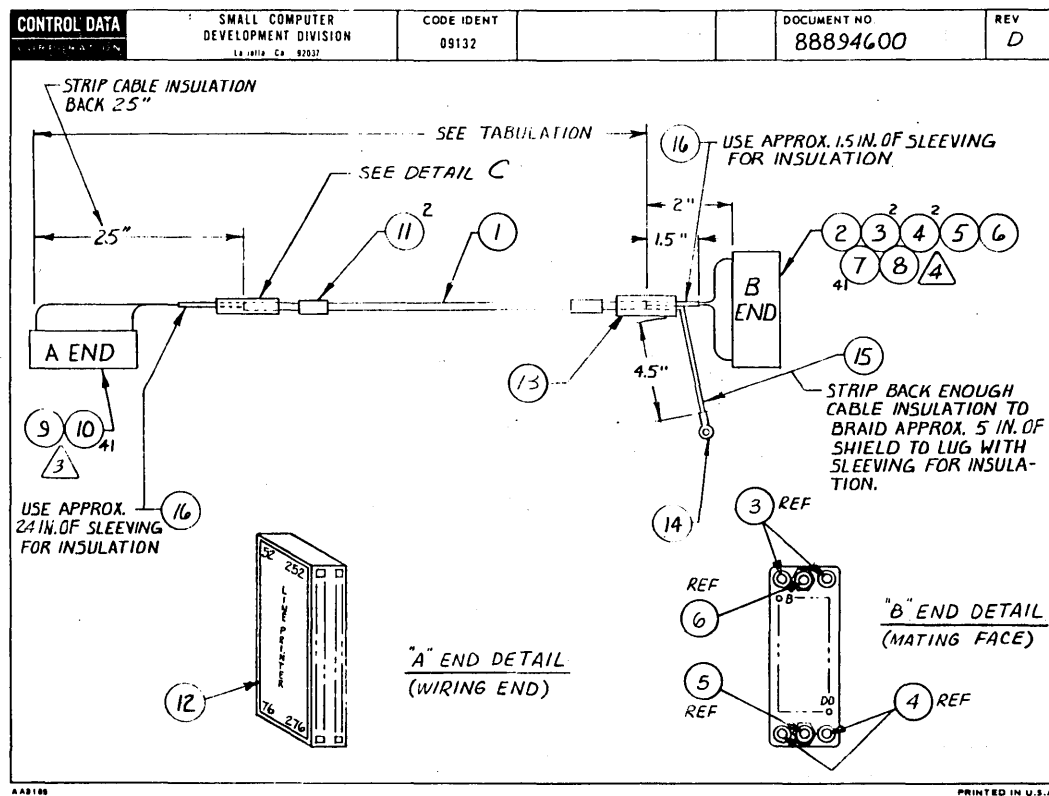
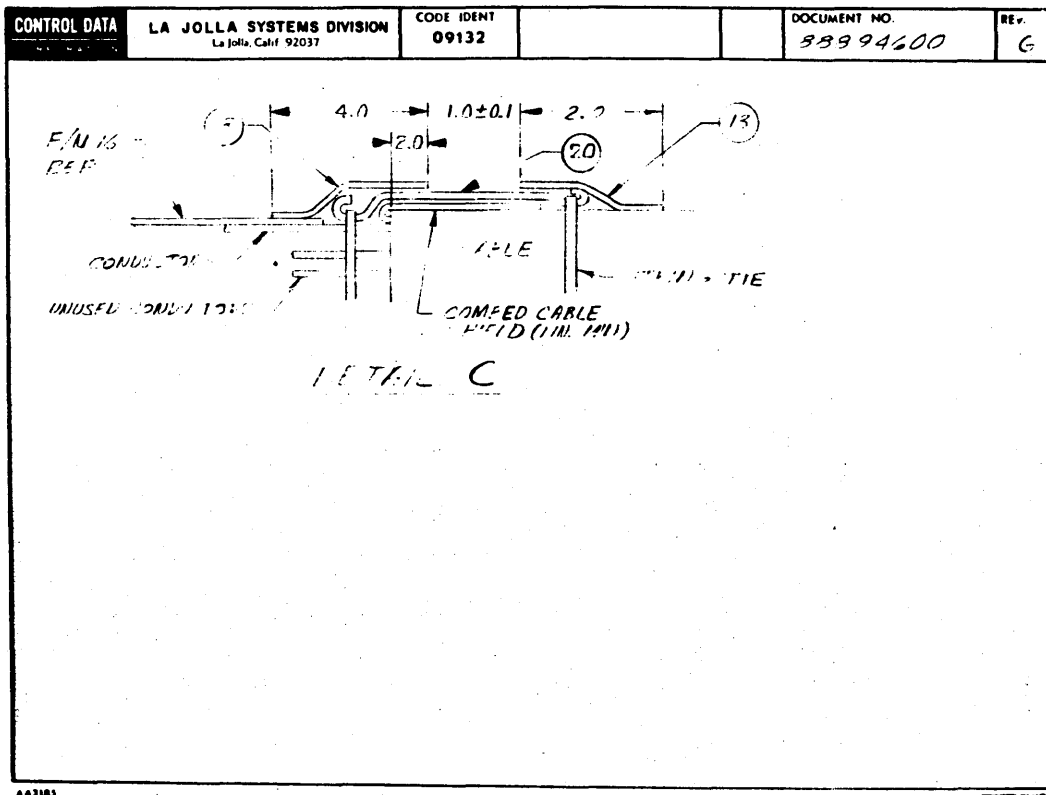


Figure 7-4. I/O Line Printer Cable Assembly (88894600) (Sheet 1 of 4)



CONTROL DATA CORPORATION		SMALL COMPUTER DEVELOPMENT DIVISION LA JOLLA, CALIF. 92037		CODE IDENT 09132		WL		DOCUMENT NO 88894600		REV D	
LINE NO.	FIND NO.	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX.)	ORIGIN	ACCESS FIND NO.	DESTINATION	ACCESS FIND NO.	REMARKS		
1	1	24	0		A-END	256	B-END	B	TWISTED PAIR (TYP)		
2			9			253		A			
3			2			66		E			
4			9			68		F			
5			4			64		H			
6			9			62		J			
7			5			273		K			
8			9			275		L			
9			6			63		M			
10			7			262		N			
11			10			69		P			
12			9			269		R			
13			91			61		S			
14			9			263		T			
15			92			270		U			
16			9			70		V			
17			93			267		W			
18			9			67		X			
19			94			255		Q			
20	1	24	9		A-END	252	B-END	b	7		

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Figure 7-4. I/O Line Printer Cable Assembly (88894600) (Sheet 2 of 4)

DWN	11-9-53	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO	REV	
CHKD	11-9-53	11-9-53	CABLE, I/O LINE PRINT (MPI7)	PL	88894600	G	
ENG	11-9-53	11-9-53	FIRST USED ON				
MFG							
APPR							
SHEET REVISION STATUS			REVISION RECORD				
			REV	ECO	DESCRIPTION	DFT	DATE
					CL B PRE-RELEASED	D.M.	11-14-75
			12	DDC	ADDED PART NO.5 (ECR4996)	D.M.	11-14-75
			13	DDC	ADDED PART NO. (FCR5001)	D.M.	11-12-75
			14	DDC	ADDED TAB 01,02,03 (ECR5002)	D.M.	11-2-76
			15	13176	ADDED IO COMMAND	D.M.	12-19-76
			16	13178	ADDED PART NO'S	D.M.	12-19-76
			17	13204	HAND F/N 1	D.M.	12-19-76
			A	13244	CL A RELEASE	D.M.	4-17-79
			B	13526	REV. SH 2 & P/L	D.M.	3-7-75
			C	14176	ADDED NOTE 2 AND F/N 17-19	D.M.	12-25-75
			D	14232	REVISED PER ECO ADDED SH 3 - BELUMBERSH	D.M.	11-10-75
			E	14341	ADDED 1/21, CHGD. NOTE 2	D.M.	3-10-76
			F	14512	SEE ECO	D.M.	3-26-76
			G	DS21211	SEE ECO	D.M.	1-1-77
NOTES:							
			DETACHED LISTS				

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Figure 7-4. I/O Line Printer Cable Assembly (88894600) (Sheet 4 of 4)

TABULATION			REVISION RECORD						
PART NO.	LG/IN	TOL±	REV	ECO	DESCRIPTION	DRAFT	DATE	CHKD	APP
96870921	240	10	A	DS19176	CL. A. RELEASED	EB	8-16-79		GB
96870922	360	14	B	DS21759	SEE ECO	CJB	10-3-79		AW
96870923	480	19	C	DS22027	ADDED NOTE 10 & TABLE 1	YB	12-16-80		AW
96870924	600	24							

NOTES CONT'D SH 2

3. SOLDER UNUSED PAIRS AT "A" END TOGETHER, SLEEVE WITH 1 IN. F/N 6, RUN ONE 16 IN. WIRE (F/N 5) TO PIN 76.

2. BAG U-CLAMP (F/N 22) AND ATTACH TO CABLE.

1. IDENTIFY PER CDC STD 1.30.008.

NOTES:

INACTIVE

INTER-DIVISIONAL DOCUMENT Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.	OWN	E. B. B.	5-5-79	CONTROL DATA DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	TITLE CABLE ASSY - I/O LINE PRINTER (CY18)				
	CHKD	L. B. B.	7-2-79		CODE IDENT 09132	A	DWG NO 96870921/24		
	ENG	L. B. B.	7-2-79						
	MFG	P. B. B.	7-17-79						
	APP								
			SCALE						

AA6030 TD

GD	DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132		DOCUMENT NO. 96870921/24	REV. C
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NOTES CONT'D :

4. SOLDER UNUSED PAIRS AT "B" END TOGETHER, SLEEVE WITH 1 IN. F/N 6, RUN ONE 3 IN. WIRE F/N 5 TO PIN X.

5. AT "B" END, STRIP BACK 6.5 IN. OF INSULATION; BRAID AND SLEEVE (WITH F/N 23) APPROX 6.25 OF SHIELD. THEN CUT ALL WIRES (NOT THE SHIELD) LEAVING 3.5 IN. PROTRUDING PAST THE OUTER JACKET.

6. FOLD END OF BRAIDED SLEEVING (F/N 21) INWARD TO FORM "FISHMOUTH"; FASTEN THIS END CLOSE TO SHRINK SLEEVING WITH CABLE TIE. THEN FORM FISHMOUTH AT OTHER END, AND STRETCH AND SMOOTH THE SLEEVING DOWN ITS ENTIRE LENGTH TOWARDS THE "A" END. BEFORE TIE WRAPPING THAT END, CHECK FOR 2 IN. SPACING AND ADJUST AS NECESSARY THE AMOUNT OF SLEEVING FOLDED INTO THE FISHMOUTH.

7. FILL ALL UNUSED CAVITIES OF F/N 18 WITH CRIMPED CONTACTS (F/N 15).

8. INSTALL LABEL (F/N 10) AFTER WIRING IS COMPLETED.

9. FILL ALL UNUSED CAVITIES OF F/N 1 WITH CRIMPED CONTACTS (F/N 14).

10. UNLESS OTHERWISE SPECIFIED ALL NOMINAL DIMENSIONS COMPLY WITH TABLE 1.

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Figure 7-5. I/O Line Printer Cable Assembly (96870921) (Sheet 1 of 4)

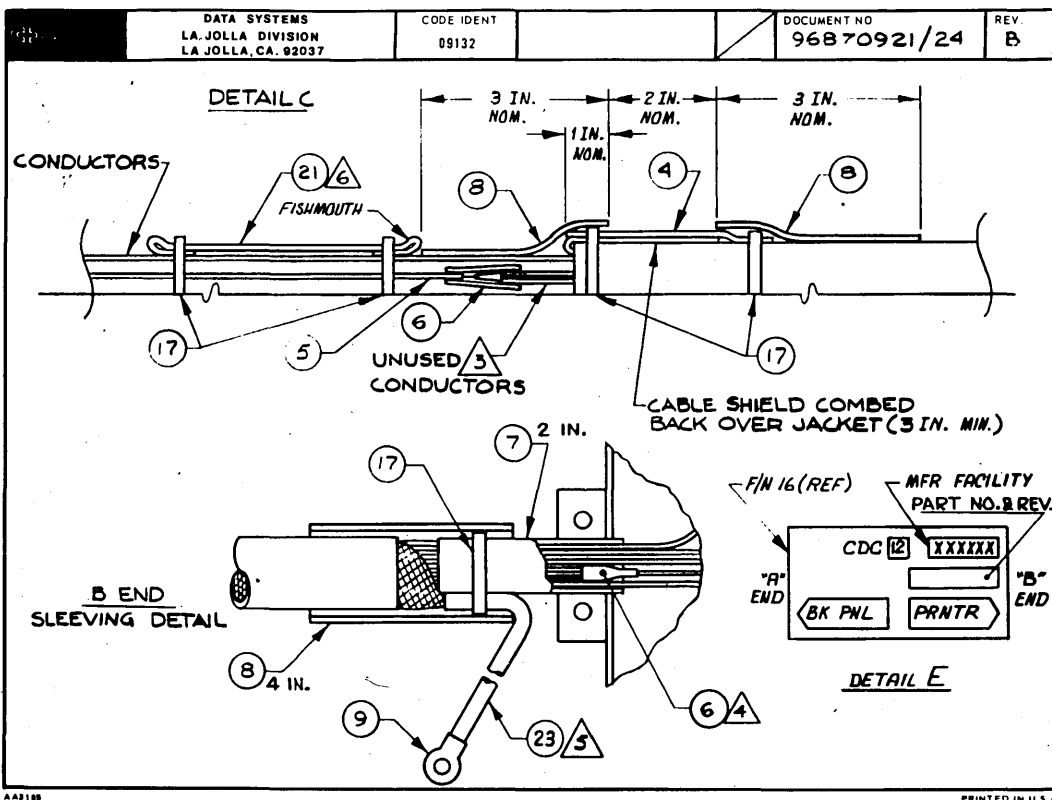
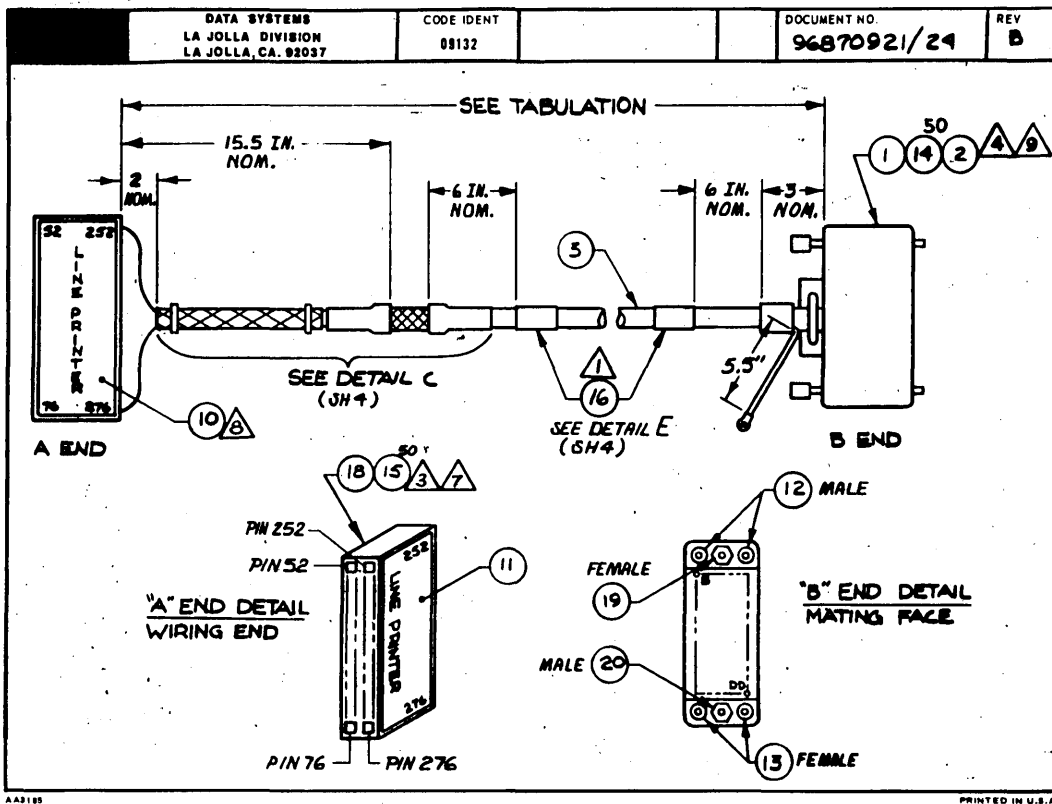


Figure 7-5. I/O Line Printer Cable Assembly (96870921) (Sheet 2 of 4)

CONTROL DATA					SMALL COMPUTER DEVELOPMENT DIVISION LA 10110 Ca 92037		CODE IDENT 09132		WL		DOCUMENT NO 96870921/24		REV 2
CONDUCTOR IDENT	FIND NO	GAUGE (REF 1)	COLOR (REF 1)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS		
1	1	24	0		A-END	258	15	B-END	B	14	TWISTED PAIR (TYP)		
2	↑	↑	9		↑	253	↑	↑	A	↑			
3			2			62			E				
4			9			63			F				
5			4			64			H				
6			9			62			J				
7			5			273			K				
8			9			275			L				
9			6			63			M				
10			9			262			N				
11			90			69			P				
12			9			269			R				
13			91			61			S				
14			9			263			T				
15			92			270			U				
16			9			70			V				
17			93			267			W				
18			9			67			X				
19	↓	↓	94		↓	255	↓	↓	a	↓			
20	1	24	9		A-END	252	15	B-END	b	14			

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CONTROL DATA					SMALL COMPUTER DEVELOPMENT DIVISION LA 10110 Ca 92037		CODE IDENT 09132		WL		DOCUMENT NO 96870921/24		REV
CONDUCTOR IDENT	FIND NO	GAUGE (REF 1)	COLOR (REF 1)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS		
21	1	24	95		A-END	274	15	B-END	c	14			
22	↑	↑	9		↑	276	↑	↑	d	↑			
23			96			254			f				
24			9			256			e				
25			97			54			p				
26			9			257			n				
27			98			259			D				
28			9			58			C				
29			900			56			j				
30			9			59			h				
31			910			53			m				
32			9			55			k				
33			920			265			s				
34			9			65			r				
35			930			260			u				
36			9			261			t				
37			940			60			w				
38			9			57			v				
39	↓	↓	950		↓	264	↓	↓	AA	↓			
40	1	24	9		A-END	266	15	B-END	z	14			

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Figure 7-5. I/O Line Printer Cable Assembly (96870921) (Sheet 3 of 4)

[illegible]

Figure 7-5. I/O Line Printer Cable Assembly (96870921) (Sheet 4 of 4)

TABULATION			REVISION RECORD						
PART NO.	LG/IN	TOL ±	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
96870925	240	10	A	DS19381	CL A. RELEASED	J.V.W.	9-30-82	<i>[Signature]</i>	<i>[Signature]</i>
96870926	360	14							
96870927	480	19							
96870928	600	24							
96870929									

NOTES:

1. MARK CABLE LABEL (F/N11) WITH PART NO. AND REVISION, PER CDC STD. 1.30.008.
2. BAG U-CLAMP (F/N 22) AND ATTACH TO CABLE.
3. SOLDER UNUSED PAIRS AT "A" END TOGETHER, SLEEVE WITH 1 IN. (F/N 5), RUN ONE 16 IN. WIRE (F/N 8) TO PIN 76.
4. SOLDER UNUSED PAIRS AT "B" END TOGETHER, SLEEVE WITH 1 IN. (F/N 5), RUN ONE 3 IN. WIRE (F/N 8) TO PIN X.

NOTES CONTINUED ON SHEET 2

DWN	CHKD	ENG	MFG	APP	DATE	TITLE
<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>	9-30-82	CABLE ASSY - I/O LINE PRINTER (CY18)
						DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037
						CODE IDENT 09132
						DWG No 96870925 THRU 96870929
						SCALE

 DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037	CODE IDENT 09132	DOCUMENT NO 96870925/29	REV A
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NOTES CONTINUED:

5. AT "B" END, STRIP BACK ENOUGH INSULATION TO BRAID APPROX. 2.5 IN. OF SHIELD; THEN SLEEVE WITH 2.25 IN. (F/N 4) AND CONNECT AS SHOWN.
6. FOLD END OF BRAIDED SLEEVING (F/N 20) INWARD TO FORM "FISHMOUTH"; FASTEN THIS END CLOSE TO SHRINK SLEEVING WITH CABLE TIE. THEN FORM FISHMOUTH AT OTHER END, AND STRETCH AND SMOOTH THE SLEEVING DOWN ITS ENTIRE LENGTH TOWARDS THE "A" END. BEFORE TIE WRAPPING THAT END, CHECK FOR 2 IN. SPACING AND ADJUST AS NECESSARY THE AMOUNT OF SLEEVING FOLDED INTO THE FISHMOUTH.
7. FILL ALL UNUSED CAVITIES OF (F/N 17) WITH CRIMPED CONTACTS (F/N 16).
8. INSTALL LABEL (F/N 9) AFTER WIRING IS COMPLETED.
9. FILL ALL UNUSED CAVITIES OF (F/N 2) WITH CRIMPED CONTACTS (F/N 15).
10. UNLESS OTHERWISE SPECIFIED ALL NOMINAL DIMENSIONS COMPLY WITH TABLE 1.

Figure 7-6. I/O Line Printer Cable Assembly (96870925/29) (FCC EMI Qualified) (Sheet 1 of 4)

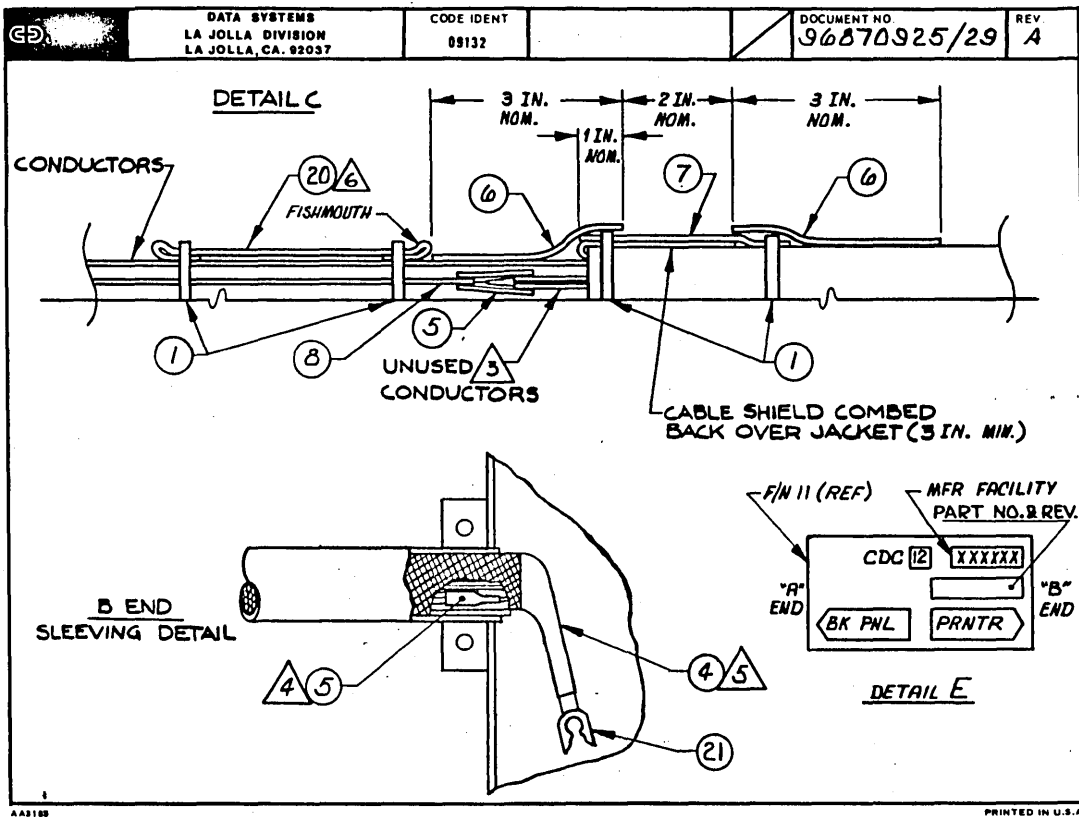
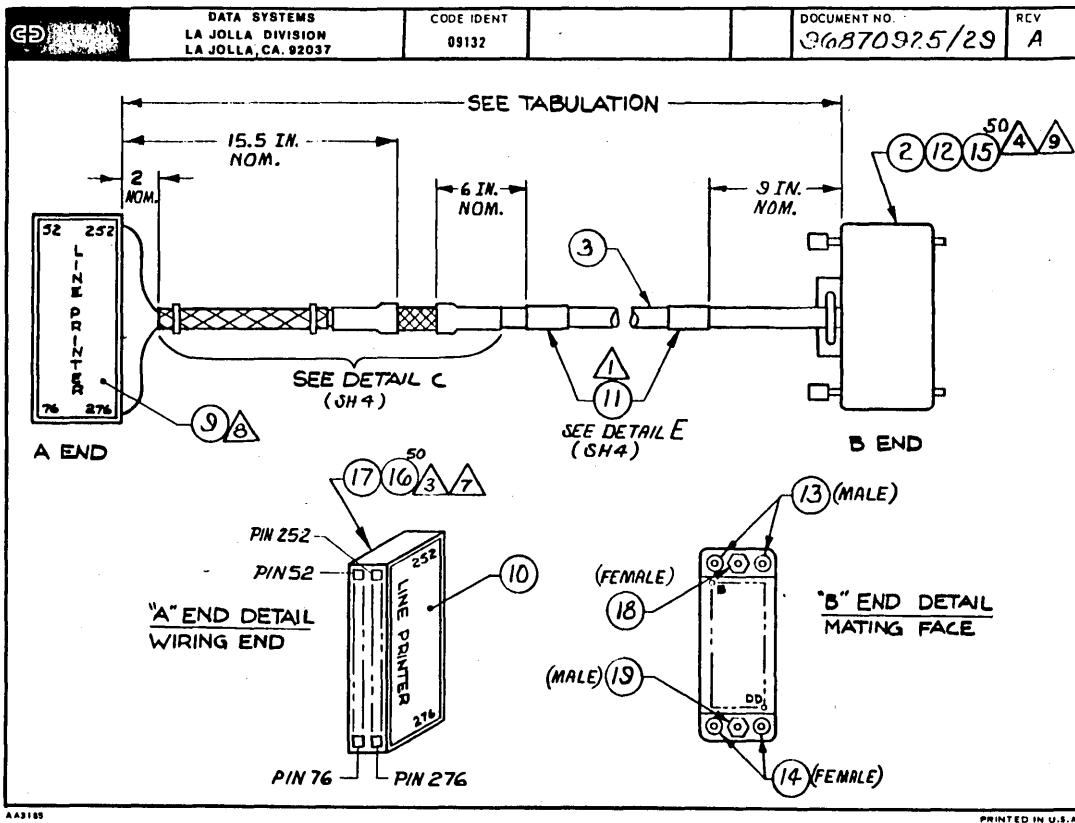


Figure 7-6. I/O Line Printer Cable Assembly (96870925/29) (FCC EMI Qualified) (Sheet 2 of 4)

DATA SYSTEMS LA JOLLA DIVISION LA JOLLA, CA. 92037		CODE IDENT 09132	DOCUMENT NO 96870925/29	REV A
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NOMINAL DIMENSION TOL TABLE			
(DIM INCHES)			TOL (INCHES)
0.5	TO	5.99	-0 +0.5
6.0	THRU	12.99	-0 +1.0
13.0	THRU	48.99	-0 +2.0
49.0	THRU	96.99	-0 +4.0
97.0	-AND UP		-0 +5.0


 TABLE 1

AA3185

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CONTROL DATA LA JOLLA DIVISION		SMALL COMPUTER DEVELOPMENT DIVISION LA JOLLA, CA. 92037			CODE IDENT 09132	WL	DOCUMENT NO 96870925/29	REV A
---	--	--	--	--	---------------------	----	----------------------------	----------

CONDUCTOR IDENT.	FIND NO	GAUGE (REF.)	COLOR (REF.)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO	DESTINATION		ACCESS FIND NO	REMARKS
1	3	24	0		A-END	258	16	B-END	B	15	TWISTED PAIR (TYP)
2	↑	↑	9		↑	253	↑	↑	A	↑	
3	↑	↑	2		↑	66	↑	↑	E	↑	
4	↑	↑	9		↑	68	↑	↑	F	↑	
5	↑	↑	4		↑	64	↑	↑	H	↑	
6	↑	↑	9		↑	62	↑	↑	J	↑	
7	↑	↑	5		↑	273	↑	↑	K	↑	
8	↑	↑	9		↑	275	↑	↑	L	↑	
9	↑	↑	6		↑	63	↑	↑	M	↑	
10	↑	↑	9		↑	262	↑	↑	N	↑	
11	↑	↑	90		↑	69	↑	↑	P	↑	
12	↑	↑	9		↑	269	↑	↑	R	↑	
13	↑	↑	91		↑	61	↑	↑	S	↑	
14	↑	↑	9		↑	263	↑	↑	T	↑	
15	↑	↑	92		↑	270	↑	↑	U	↑	
16	↑	↑	9		↑	70	↑	↑	V	↑	
17	↑	↑	93		↑	267	↑	↑	W	↑	
18	↑	↑	9		↑	67	↑	↑	X	↑	
19	↓	↓	94		↓	255	↓	↓	Q	↓	
20	3	24	9		A-END	252	16	B-END	b	15	

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Figure 7-6. I/O Line Printer Cable Assembly (96870925/29) (FCC EMI Qualified) (Sheet 3 of 4)

COMMENT SHEET

MANUAL TITLE: CDC® FH301-A Card Reader/Line Printer Controller
Hardware Reference/Maintenance Manual

PUBLICATION NO.: 96728800

REVISION: E

NAME: _____

COMPANY: _____

STREET ADDRESS: _____

CITY: _____ STATE: _____ ZIP CODE: _____

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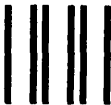
FOLD ON DOTTED LINES AND TAPE

STAPLE

STAPLE

OLD

FOLD



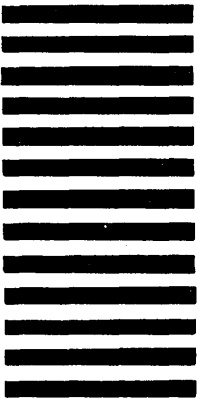
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